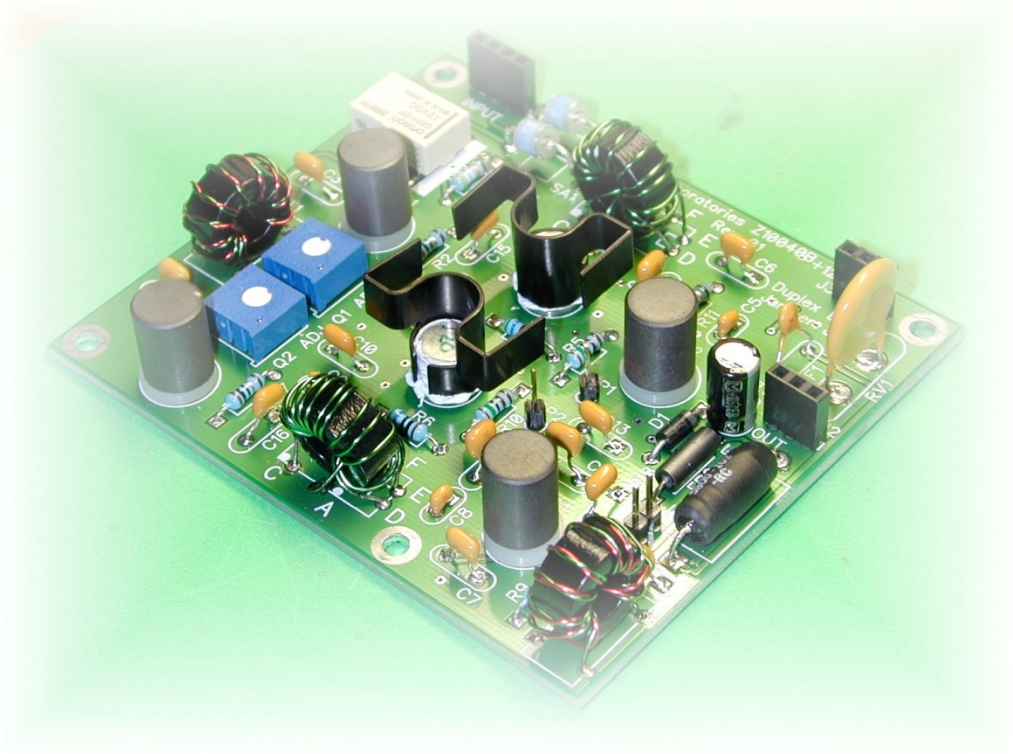
Z10040B
Broadband Norton Amplifier

Assembly and Operation Manual



Version 1.6.1 April 2010

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Model Z10040B Broadband Norton Amplifier

Version 1.6.1 2010

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Last Revised 04 April 2010

Trademarks and Copyright

Material in this document copyrighted © 2010 Clifton Laboratories. All rights reserved. It is provided to allow the Z10040B purchasers to maintain their equipment and such other purposes as may not be prohibited by law.

Warranty

This warranty is effective as of the date of first consumer purchase.

What is covered: During the ninety (90) days after date of purchase, Clifton Laboratories will correct any defects in the Z10040B due to defective parts or workmanship (if purchased as an assembled unit) free of charge (post-paid). You must send the unit at your expense to Clifton Laboratories, but we will pay return shipping. Clifton Laboratories' warranty does not extend to defects caused by your incorrect assembly or use of unauthorized parts or materials or construction practices.

What is not covered: If the Z10040B is purchased as a kit, this warranty does not cover correction of assembly errors or misalignment; repair of damage caused by misuse, negligence, or builder modifications; or any performance malfunctions involving non-Clifton Laboratories accessory equipment. *The use of acid-core solder, water-soluble flux solder, or any corrosive or conductive flux or solvent will void this warranty in its entirety.* Damage to the Z10040B or equipment connected to it caused by lightning strikes is not covered under the warranty. Whether purchased as an assembled unit or as a kit, also not covered is reimbursement for loss of use, inconvenience, customer assembly or alignment time, or cost of unauthorized service.

Limitation of incidental or consequential damages: This warranty does not extend to non-Clifton Laboratories equipment or components used in conjunction with our products. *Any such repair or replacement is the responsibility of the customer. Clifton Laboratories will not be liable for any special, indirect, incidental or consequential damages, including but not limited to any loss of business or profits.*

Under no circumstances is Clifton Laboratories liable for damage to your equipment connected to the Z10040B resulting from use of the Z10040B, whether in accordance with the instructions in this Manual or otherwise.

Safety Information

The Z10040B operates with a user-supplied DC power supply of 13 to 15 Volts at 100 to 120 mA. The Z10040B, although designed as a low signal level preamplifier, is capable of RF output power approaching the 1 watt level. This output power is capable of damaging receivers or the receiver section of a transceiver or test equipment. It is the user's responsibility to ensure that the Z10040B is properly connected to whatever devices it will be used with.

The Z10040B has no replaceable fuses; rather a self-resetting polyfuse limits short circuit current to approximately 200 mA.

The Z10040B is designed to be used only with receive-type power levels. It should not be used with transmitting equipment. The Z10040B's maximum permitted input RF power is 100 mW (+20 dBm). *Power in excess of this level may damage the Z10040B or equipment connected to it, or both. In addition, since the Z10040B has appreciable gain, output power levels sufficient to damage connected equipment may occur with input signal levels well below +20 dBm.*

Although the Z10040B contains protective measures, all of these protection measures assume that the Z10040B is properly grounded and that good engineering practices have been used in its installation and construction of the ground system. The Z10040B is not intended to survive a direct lightning strike to an antenna connected to its input, whether powered up or not. However, the protective measures incorporated into the Z10040B's design should aid in reducing damage.

General Information and Specifications

Description

The term "Norton Amplifiers" refers to a class of transformer feedback amplifiers developed by Dr. David Norton and described in his US Patent No. 3,891,934, granted June 24, 1975 and now in the public domain. (A copy of Dr. Norton's patent is Appendix C to this Manual.) A Norton amplifier permits the distortion reducing benefits of negative feedback to be applied without impairing the amplifier's noise figure. Hence, Norton amplifiers are also known as "noiseless feedback" amplifiers.

The Z10040B is a broadband (75 KHz to 30 MHz) Norton-style amplifier providing 11 dB gain (other gain values are possible) with very high 3rd order and 2nd order intermodulation intercepts, IP3 and IP2, respectively, with a noise figure below 3.5 dB over the range 10-30 MHz. The Z10040B is designed for either indoor or outdoor use, with DC power supplied through either separate connections or duplexed over the output coaxial cable. Optional indoor and outdoor die cast enclosures are available for the Z10040B.

The Z10040B is derived from the Norton Amplifier developed by Dr. Dallas Lankford and described in his publication *Common Base Transformer Feedback Norton Amplifiers*, dated 8 June 1994, revised 21 May 2007, available at http://www.kongsfjord.no/dl/Amplifiers/Common%20Base%20Transformer%20Feedback%20Norton%20Amplifiers.pdf.

The Z10040B modifies Dr. Lankford's design in several respects:

- Automatic input disconnect upon DC power removal along with over-voltage gas trap protection
- Improved performance below 500 KHz.
- Over voltage and reverse voltage protection on the DC Power.
- DC power either separately or duplex power.
- Optional balanced or unbalanced input.

Clifton Laboratories also offers the Z1203A DC power injector usable with the Z10040B to provide DC power over the coaxial cable.

The Z10040B is available as a kit, including a double sided, silk screened solder masked printed circuit boards and all electronic parts or as an assembled and tested printed circuit board. Options include an indoor die cast enclosure or an outdoor weatherproof die cast enclosure with BNC, UHF or Type N connectors.

Typical kit construction time is three to five hours depending on your work practices. The kit is suitable for relatively inexperienced builders, although Clifton Laboratories does not recommend it to purchasers who have never built an electronic kit before. Also, if you have never wound a toroid inductor or transformer, you might wish to ask an experienced builder to show you how it's done.

Specifications

Parameter	Value
PCB Dimensions	3.00” x 3.50” x 0.75” vertical clearance required. (76.2mm x 88.9mm x 19mm). Four mounting holes for 4-40 screws provided, template in Appendix B.
DC Power Required	Maximum: 15V Minimum: 13.8V [may not meet specifications below this voltage. See Appendix D for performance versus supply voltage considerations.] Negative to ground, typical DC current 80-100 mA depending on bias adjustment.
Maximum RF Power Input	Do not exceed 100 milliwatts (+20 dBm). IP3 performance specifications are based upon -10 dBm signal input; performance not warranted at greater input levels.
Test Conditions	Performance data is for a 1:11:4 turns ratio design, 13.8 VDC after adjusting balance trimpots for minimum 2nd harmonic distortion. Unless otherwise indicated, performance measurements are made with direct DC power, not duplexed. Figures stated as “typical” are not warranted.
3 dB Bandwidth	100 KHz – 30 MHz. Typical bandwidth 75 KHz - 45 MHz
2nd and 3rd Order Intermodulation Intercept	Measured with 3 and 4 MHz input tones, adjusted for 0 dBm output from the Z10040B. Protocol as discussed later in this manual. Intercepts are output referenced. OIP2: +80 dBm OIP3: +45 dBm
Gain	11 dB nominal at 1 MHz.
1 dB Gain Compression	+19 dBm input.
Noise Figure	3.5 dB maximum 10-30 MHz. Typically less than 3 dB 10-30 MHz.
Input VSWR	When terminated with 50 ohm load, input VSWR is less than 2:1 over the range 300 KHz – 30 MHz, and is typically below 1.5:1 over this range.
Common Mode Rejection in Balanced Input Mode	Typically 50 dB at 1 MHz, decreases with increasing frequency.

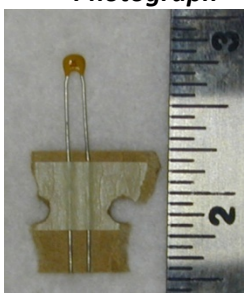
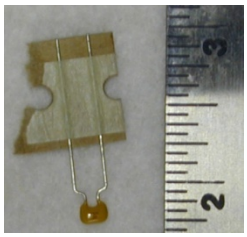
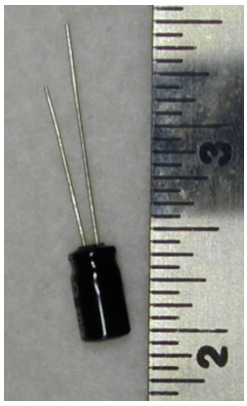
Assembly

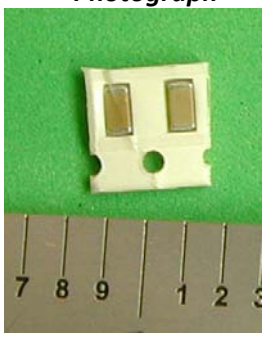
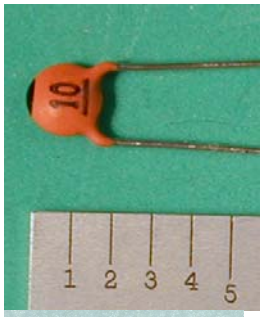
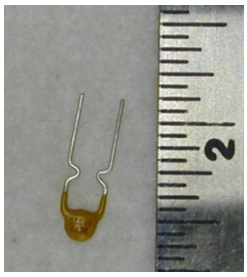
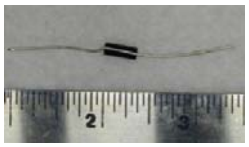
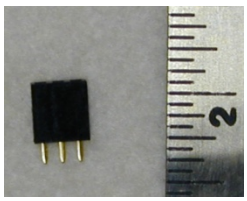
Parts Provided

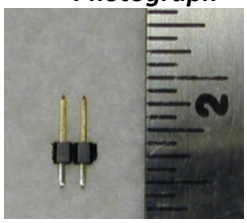
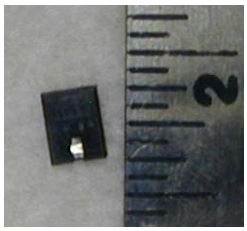
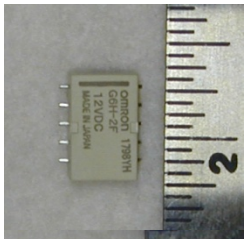
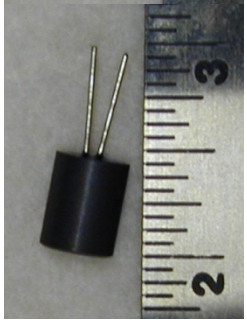
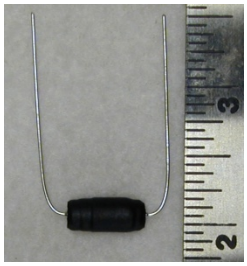
Before starting your build, please take a moment and inventory the parts provided against the list below. The ruler is marked in inches and and 1/16th fractions (some photos use a ruler marked in inches and tenths, identified at 10 THS.).

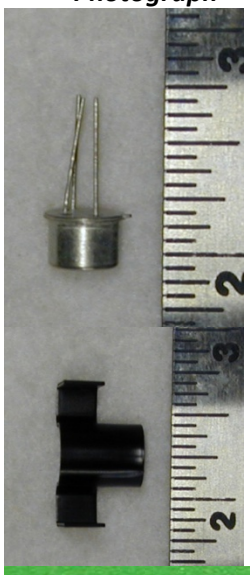
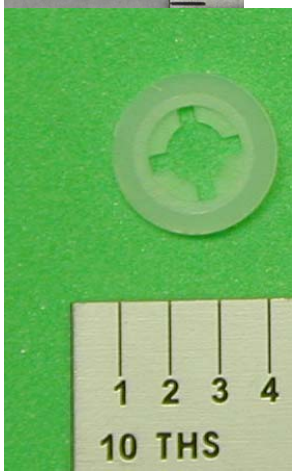
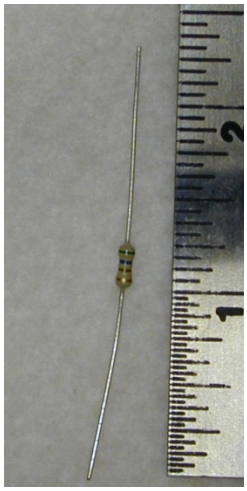
A note on how component values are identified in this manual

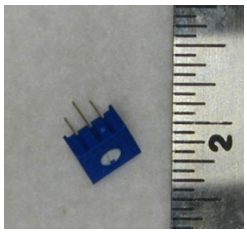
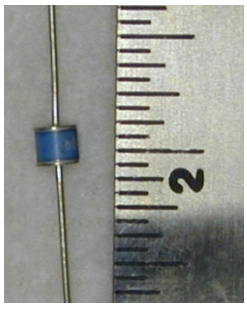
This document follows the international practice of using the value multiplier to indicate the decimal point. Thus, a 1.0µF capacitor is identified as 1µ0 and a 10,000 ohm resistor is identified as 10K0.

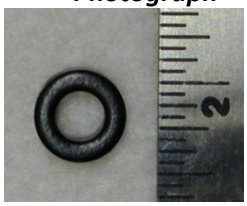
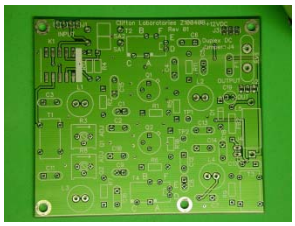
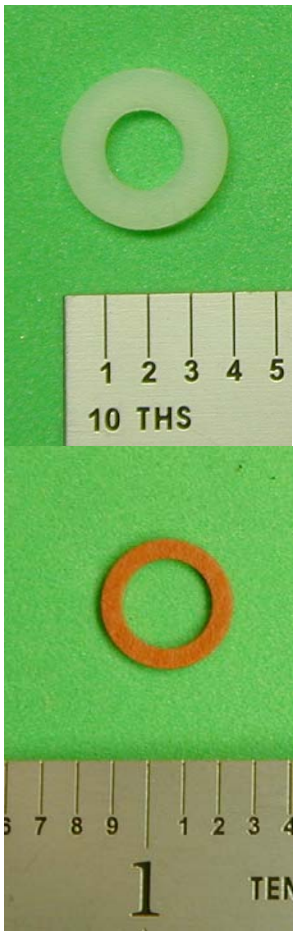
Photograph	*Qty*	*ID*	*Description and Comments*	*Component Marking*
	4	C1, C5, C8, C9	1000pF leaded ceramic capacitor. Lead spacing 0.1 inches. Parts may be loose or taped as shown.	102
	14	C10, C11, C12, C13, C14, C15, C16, C17, C18, C2, C3, C4, C6, C7	1u0 leaded ceramic capacitor. Lead spacing 0.2 inches. Parts may be loose or taped as shown and may or may not have a "crimped" lead.	105
	1	C19	33u 63V electrolytic capacitor. This component is polarized. Polarity is identified by two methods. The negative lead is the shorter one and the negative lead is marked with a negative symbol on the capacitor case. The longer lead is the positive lead.	33uF 63V

Photograph	*Qty*	*ID*	*Description and Comments*	*Component Marking*
	2	C20, C21	100 pF, 1206 surface mount ceramic capacitor. (Photo shows capacitors still inside the paper tape.)	none
	2	C22, C23	10pf disc ceramic capacitor	10
	1	D1	Silicon diode, 1A or greater, 100V or greater. Typically a 1N4007 part	1N400x where X may be any number from 0 to 7
	1	F1	200 mA Raychem “polyfuse” PTC varistor. The supplied part may or may not have a “crimped” lead.	XF020
	1	FB2	Ferrite bead [FB1 designator is not used]	No marking
	2 [3-place] 1 [4-place]	J1, J2, J3	J1: 4-place J2 & J3: 3 place 0.1 inch header sockets	None

Photograph	*Qty*	*ID*	*Description and Comments*	*Component Marking*
	1	J4	2 place 0.1 inch header pin May be supplied as a multiple pin strip to be broken as needed by builder	None
	1	None	Shorting jumper for 2 place 0.1 inch header pins	None
	1	K1	G6H-2F-DC12 double pole, double throw 12V surface mount relay	G6H-2F-12VDC
	4	L1, L2, L3, L4	1m0 RF choke (shielded) high current	None
	1	L5	1m0 RF choke, high current unshielded	5800-102

Photograph	*Qty*	*ID*	*Description and Comments*	*Component Marking*
	2	Q1, Q2	NPN transistors, VHF, type 2N5109	2N5109
	2	None	Heat sinks for Q1 and Q2	None
	2	None	Nylon insulating spacer for Q1 and Q2. Note this spacer has four serrations in the inner opening	None
	¼ watt, 1% metal film resistors These parts have five color bands: 1. 1st significant figure 2. 2nd significant figure 3. 3rd significant figure 4. Multiplier (number of zeros or N in 10^N notation) 5. Tolerance (1% = brown) Example: brown-green-black-brown-brown = 1 5 0 1 1: 150 x 10^1, 1% tolerance = 1500 ohms, ±1%			
	2	R1,R6	560R	Green-blue-black-black-brown
	2	R4,R12	49R9 *first band is yellow, but looks more like green with	Yellow*-white-white-gold-brown

Photograph	*Qty*	*ID*	*Description and Comments*	*Component Marking*
			some lighting sources	
	2	R10, R5	1K50	Brown-green-black-brown-brown
	4	R2, R7, R9,R11	10R0	Brown-black-black-silver-brown
	2	R3, R8	100R Trim-pot	101
	1	RV1	14mm dia. 18V over-voltage MOV	180M
	2	SA1, SA2	Spark gap Either of the following may be provided: 90V 75V	90V (and date code) EC 75 (and date code)
Same as J4.	2	TP1, TP2	Test points. Use header pin. May be supplied as a multiple pin strip to be broken as needed by builder	None
Same as J4	3	None	3 place header pins. May be supplied as a multiple pin strip to be broken as needed by builder	None

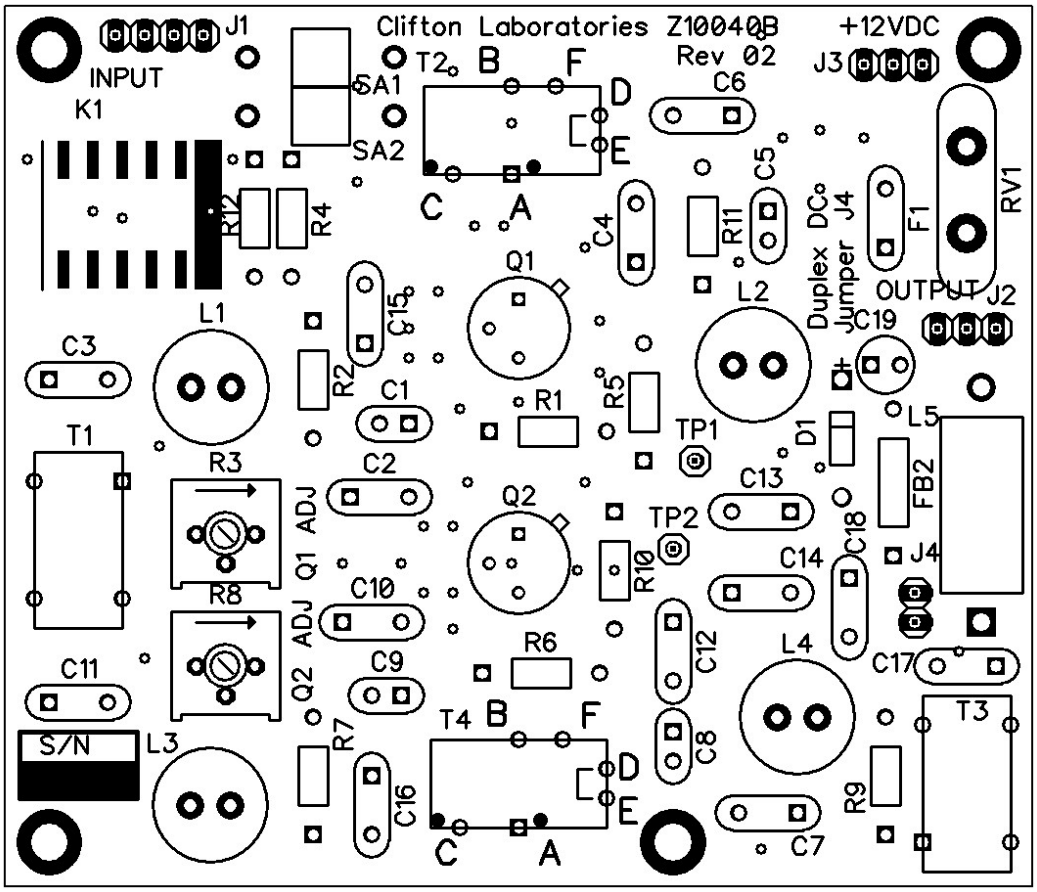
Photograph	*Qty*	*ID*	*Description and Comments*	*Component Marking*
	4	T1,T2,T3, T4	0.5 inch diameter ferrite cores; builder to wind	None
	1	PCB	Printed circuit board. Identified as Z10040B	Z10040B and revision number
None	1 length #24 wire	None	No. 24 AWG magnet wire, use for T2 and T4	None
None	2 lengths #26 wire	None	No. 26 AWG magnet wire, use for T1 and T3. One length red, one length green.	None
	4	None	Washers for L1-L4. Note these washers do not have serrations in the inner opening and are larger diameter than the two insulators for Q1 and Q2. The supplied parts may be nylon as illustrated in the upper photograph or hard fiber as in the lower photograph.	None

Photograph	*Qty*	*ID*	*Description and Comments*	*Component Marking*
None	4 inches (100mm)		Teflon insulated solid wire	None

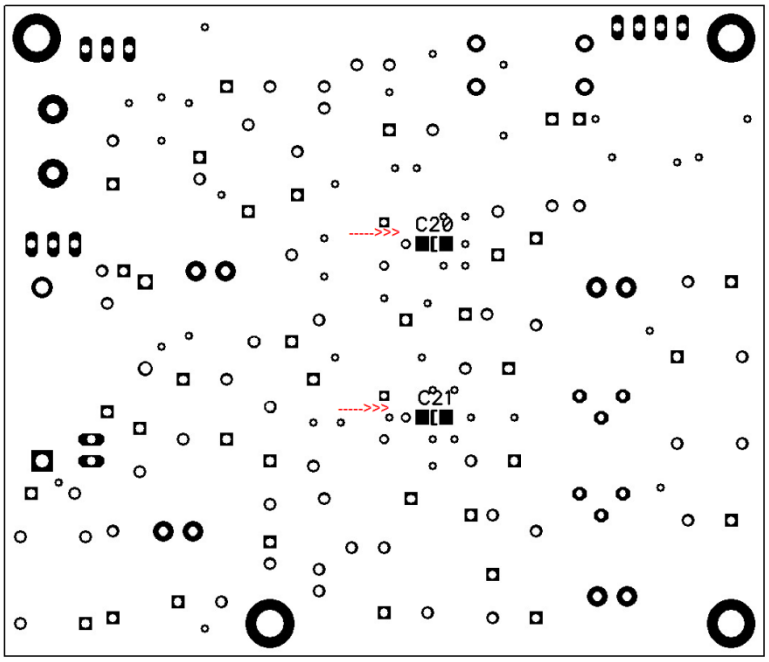
Errata:

None known for Rev 02 PCB.

Component Layout



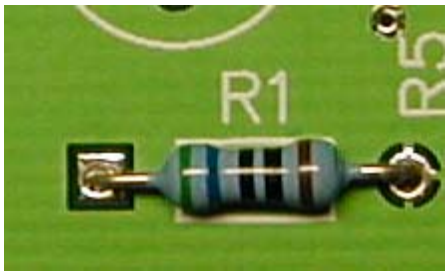
Top view



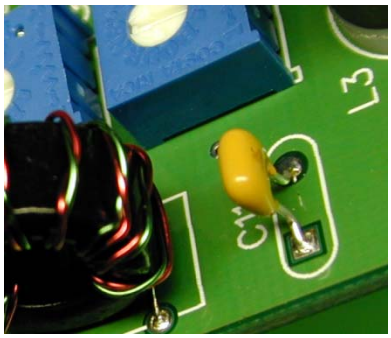
C20, C21, C22 and C23 install on the PCB bottom. There is no silk screening identifying the location for these parts.

Component Orientation

As a matter of good construction practice, most builders orient non-polarized components in the following fashion:



- If the component is color coded, such as most resistors, orient so that the color code reads in the same direction as the silk screening designator. R1, for example, is a 560 ohm 1% resistor; color coded green blue black black brown. Note that the color code is oriented so it reads left-to-right, just as the component silk screened R1 designation.
- Parts with a printed value code are oriented so that the part value may be easily read. For example, C11 is a 1u0 capacitor, marked 105. The part is installed with the printed "105" identification facing away from T1 so that the marking is more easily read.



Of course, if the component is polarized, it must be installed with the proper polarity. Even there, it may be possible to rotate the part (such as the 1N4007 diode) so that the part identifier is not obscured.

Assembly Order

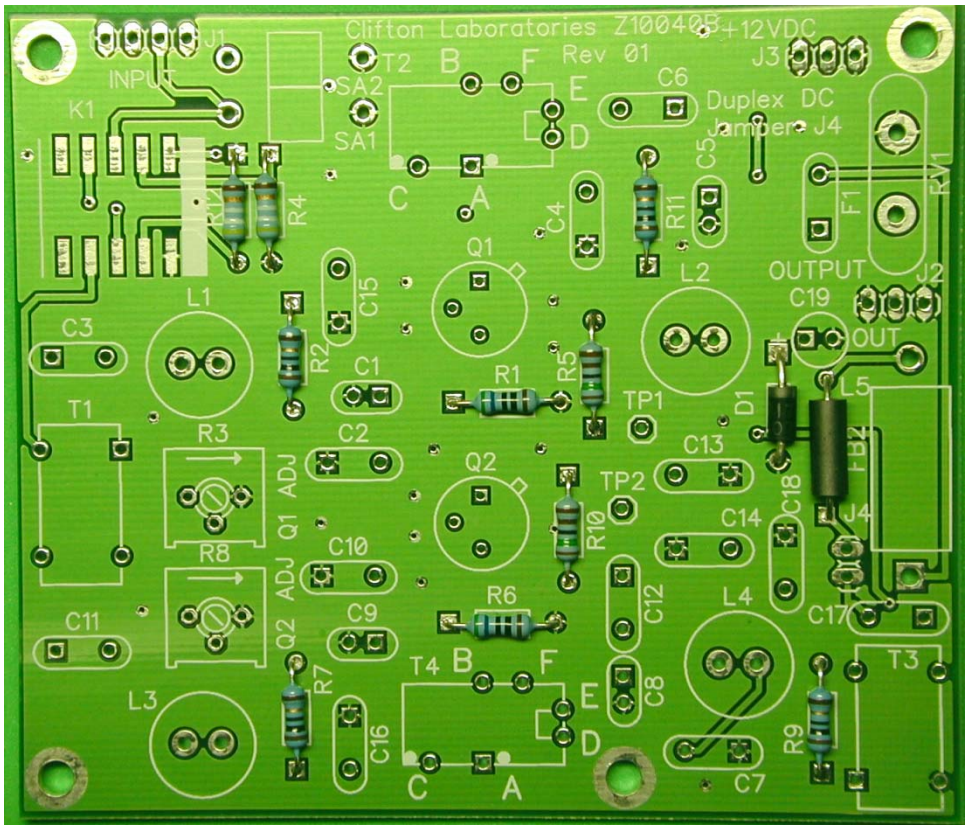
The Z10040B is a relatively simple kit. The most complex part is winding the transformers, and even this is not difficult.

The assembly order generally follows component height—the smallest components are installed first, and the transformers last. (Where there is no difference, the photos are of the rev 02 PCB.)

Install the ¼ watt 1% metal film resistors

- ❑ R1 560R green-blue-black-brown-brown
- ❑ R6 560R green-blue-black-brown-brown
- ❑ R4 49R9 yellow-white-white-gold-brown (yellow may look greenish under fluorescent lighting)
- ❑ R12 49R9 yellow-white-white-gold-brown (yellow may look greenish under fluorescent lighting)
- ❑ R5 1K50 brown-green-black-brown-brown
- ❑ R10 1K50 brown-green-black-brown-brown
- ❑ R11 10R0 brown-black-black-silver-brown
- ❑ R9 10R0 brown-black-black-silver-brown
- ❑ R2 10R0 brown-black-black-silver-brown
- ❑ R7 10R0 brown-black-black-silver-brown
- ❑ Install D1, the reverse polarity protection diode. This will be a 1N400x series device, marked 1N400x where x may by any digit from 0 to 7. Observe polarity when installing the diode; the diode body will be marked with a bar or ring around one end. The lead from the marked end goes into the pad marked with a bar and the + sign.
- ❑ Install FB2, the ferrite bead. (FB1 is not used.) The ferrite bead is not marked and is not polarity sensitive.

The photo below shows the PCB at this stage of assembly.



Install 1u0 capacitors (marked 105) at:

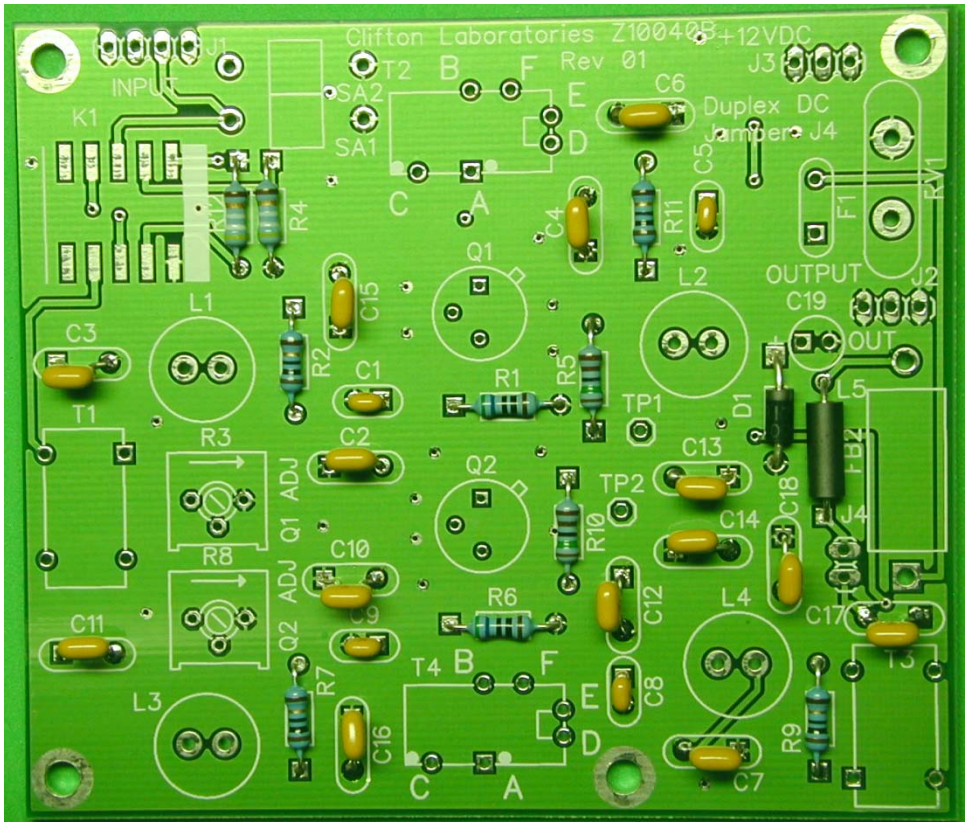
- ❑ C3
- ❑ C11
- ❑ C10
- ❑ C2
- ❑ C4
- ❑ C14
- ❑ C18
- ❑ C17
- ❑ C16
- ❑ C15
- ❑ C6
- ❑ C13

- ❑ C12
- ❑ C7

Install 1000pF capacitors (marked 102 or) at:

- ❑ C1
- ❑ C9
- ❑ C8
- ❑ C5

The photo below shows the PCB at this stage of assembly.



- ❑ Install L5, 1m0 RF choke, marked 5800-102.
- ❑ Install F1 (RXE020 200 mA polyfuse, marked XF020). Depending on the available product, this component may have parallel, crimped leads or angled leads.

To install the crimped lead version, slip one lead into the mounting hole so that the kink or crimp snaps across the PCB. Put the second lead into the other mounting hole and gently pull (with long nose pliers) the second lead from the underside of the board until it

likewise snaps into the mounting hole. If this process is too difficult, you may simply install F1 with the crimped leads above the PCB surface. Solder.

If the angled leaded device is provided, install until the bend in the lead contacts the top of the printed circuit board pad. Solder.

❑ Install RV1, the MOV over-voltage protector, marked 180M. RV1 is not polarized and may be installed in either orientation.

❑ Install R3, a 100R trimpot, marked 101.

❑ Install R8, a 100R trimpot, marked 101.



Install the four 1m0 shielded RF chokes, L1 through L4. These chokes are constructed with a ferrite cylinder for shielding and potted with epoxy. It is common for the epoxy to slightly extend beyond the shield bottom. To provide better mechanical support, install a nylon or fiber washer between the choke and the PCB as illustrated to the right. Trial fit the choke and washer in the PCB. In some cases, the epoxy will still prevent a good mechanical fit. In this case, trim or slot the inside of the nylon washer with a hobby knife, being careful not to cut yourself during the process. Alternatively, you may use the washer without trimming, accepting a small gap between the choke/washer/PCB assembly.

Recommended assembly process: Fit all four of the RF choke and washer assemblies to the PCB but do not solder. Put a small piece of flat material, such as a piece of metal or thin wood or plastic on top of all four chokes, creating a "sandwich" with the chokes as the filler and the PCB and metal the bread. Hold the sandwich together and flip the assembly upside down so that the choke leads are sticking up and place the "sandwich" on the workbench. Hold the PCB down to apply pressure to seat the choke/washer assembly against the PCB. (I use a pair of small woodworker's clamps for this purpose.) Solder <u>one lead</u> of each choke. After soldering one lead of all four chokes, pick up the PCB and verify each choke is seated as well as possible against the washer and the PCB. If any choke is not fully seated, press it against the PCB while heating the solder joint. After all chokes are fully seated, solder the remaining leads.

❑ L1

❑ L2

❑ L3

❑ L4

❑ Install the three-pin header socket (female) at J2.

❑ Install C19 (33µF, 63V electrolytic capacitor). This is a polarized part. Polarity may be indicated by either (or both) of the following: (a) The capacitor has a negative side marking; (b) the positive lead is the longest. Install C1 <u>ensuring the positive lead is inserted</u>

into the pad marked with the + sign. Solder.

❑ Locate the two 2N5109 transistors and the two nylon insulators. Note that the insulator has four notches.



Slip one insulator over each transistor, orienting it so that the three leads fit into notches.

❑ Install Q1 (marked 2N5109) with its insulator at Q1. The transistor body / insulator combination should be flush against the PCB surface. Verify that no leads have been bent and that Q1's emitter tab aligns with the silk screen tab mark before soldering.

❑ Install Q2 (marked 2N5109) with its insulator at Q2. The transistor body / insulator combination should be flush against the PCB surface. Verify that no leads have been bent and that Q2's emitter tab aligns with the silk screen tab mark before soldering.

❑ Install K1 relay, marked as G6H-2F; orient the marking bar on the relay to match the thick bar on the PCB silkscreen as shown in the photo at right. To install K1, first apply a light solder coat to one of the end pads on the PCB. Hold K1 on top of the pad and gently press down on it whilst heating the tinned pad. Check K1's alignment to verify that all pins are centered in their associated pads. Solder the diagonal pad. Recheck alignment and solder the remaining pins in place. Touch up the first pad.



❑ Install SA1, the spark gap, marked either 90V plus a date code or EC75 plus a date code. SA1 is not polarized and may be installed in either orientation. Be careful when bending the leads as the ceramic body is fragile. SA1 should be installed so that the body is approximately 1/8th inch (3 mm) above the PCB surface.

❑ Install SA2, the spark gap, marked either 90V plus a date code or EC75 plus a date code. SA2 is not polarized and may be installed in either orientation. Be careful when bending the leads as the ceramic body is fragile. SA1 should be installed so that the body is approximately 1/8th inch (3 mm) above the PCB surface.

SA1 and SA2 should not contact each other. Slightly bend SA1 or SA2 or both, if necessary to provide approximately 1/8th inch (3 mm) horizontal spacing between SA1 and SA2. Be careful when bending these parts not to over-stress SA1 and SA2's ceramic body.

Note: The silk screen legends for SA1 and SA2 are reversed in Board Rev. 01.

❑ Install the three-pin header sockets (female) at J3

❑ Install the four-pin header sockets (female) at J1

❑ Locate the header pin (male) strip and break or cut two pins from the strip. Install the two pins at J4. (The short side goes into the pad holes.)

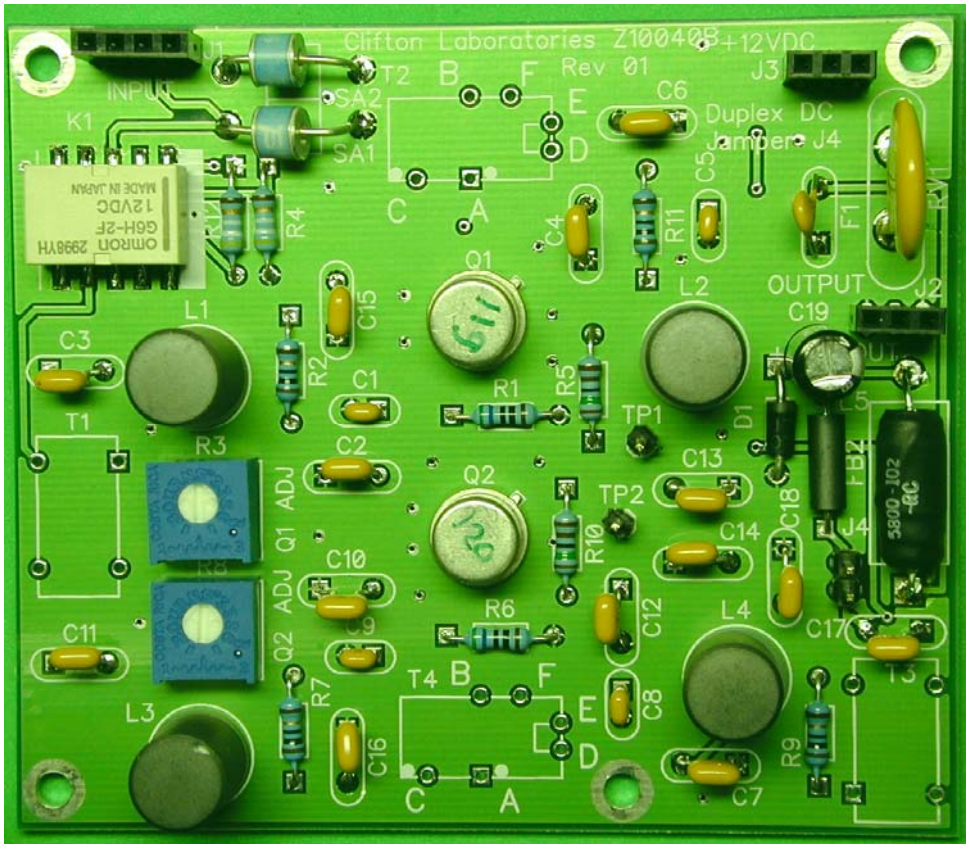
❑ Cut or break two individual pins from the header pin strip.

❑ Install one pin at TP1.

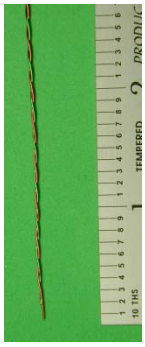
❑ Install one pin at TP2.

At this point, all components should be installed on the PCB's top surface, except for the four transformers and the two heat sinks. The two 100pF surface mount capacitors and the two 4p7 disc ceramic capacitors are installed later in the build.

The photo below shows the PCB at this stage.



❑ Locate the No. 26 AWG magnet wire. (It is the smaller diameter of the two wire sizes.) One length of green insulated wire is provided and one of red insulated wire.

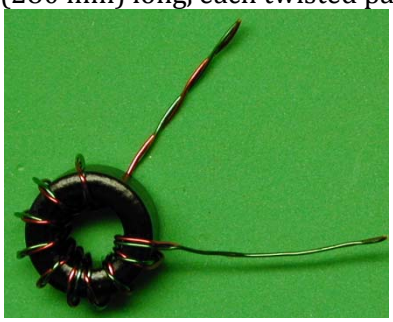


Cut four lengths of the wire:
Two pieces green, each 11 inches (280 mm) long.
Two pieces red, each 11 inches (280 mm) long.

Take one piece of red wire and one piece of green wire and twist approximately 60 turns. Repeat for the second pair of red and green wires. (A variable speed drill, running slow speed, speeds up the twisting process.)

At this point, you should have two twisted wire sections, each approximately 11 inches

(280 mm) long, each twisted pair with one red and one green wire.

❑ 

Wind the twisted wire 10 turns onto one of the ferrite cores.

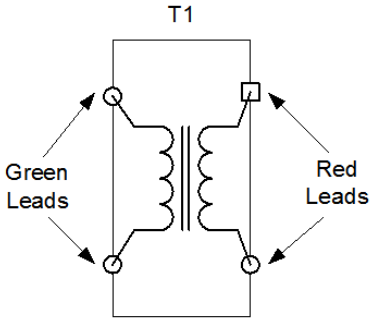
As a reminder, a turn is counted when the wire passes through the hole in the core.

Start by inserting the cut end approximately one inch (25 mm) through the core. Thread the doubled end through and wind 10 turns. Space the turns so that the windings occupy approximately 75% of the core perimeter (270 degrees if you prefer to think in those terms).

Repeat for the second transformer.

Congratulations. You have completed winding two bifilar broadband transformers, T1 and T3.

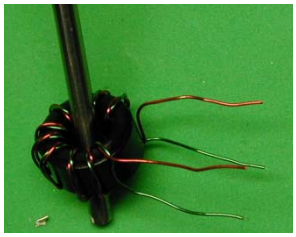
Locate the PCB and look at the silk screen outline for T1 and T3. Note that each has four pads, comprised of three round pads and one square pad, oriented as shown in the drawing.



The green wires connect to the two round pads on one side and the red wires connect to the one square and one round pad on the opposite side. [This is not critical and one can interchange the green and red leads, but troubleshooting will be easier if all the Z10040B's are built the same way.]

Un-twist the pigtails so that you have four separated wires. Remove the insulation and tin the four wires.

The wire leads should be formed as illustrated in the photo to the right. Install the transformer as shown in the drawing at T1. Note: If you do not intend to use your Z10040B with balanced input, you may wish to perform the modification described on the next page when installing T1.



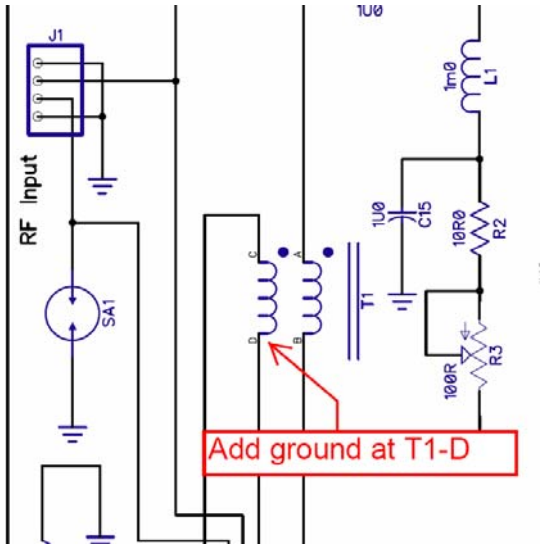
Note: The red and green wire supplied is "solderable" and the insulation will melt if heated with a blob of molten solder. This heating and tinning must be done <u>before</u> the transformers are installed in the PCB.

A common error in installing T1 and T3 (as well as T2 and T4) is that the insulation is not fully removed from the wire due to insufficient heating.

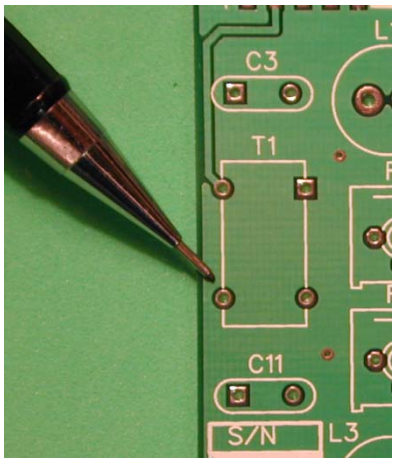
<u>Optional Modification if the Z10040B will only be used with unbalanced input.</u>

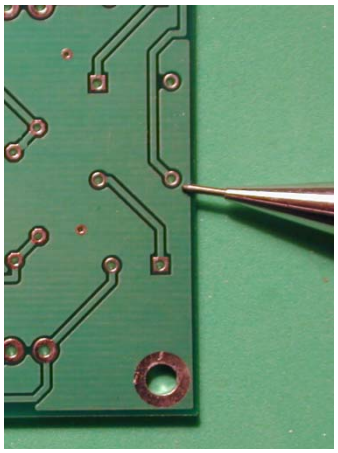
Responding to customer requests, the Z10040B added optional balanced input, with the choice between balanced and unbalanced operation being made via input plug location. If

the Z10040B is to be used only in unbalanced mode (which is likely to be the vast majority of cases) a slight improvement in performance can be observed by adding a grounding point near T1's pin "D." The top and bottom locations of T1-D are shown in the photographs.

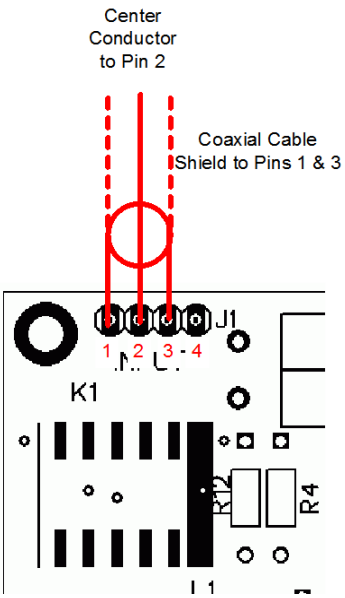


To make the modification, remove the solder mask from a small area of the printed circuit board ground plane on the bottom surface near T1-D. This may be done by gently scraping the solder mask away using a sharp hobby knife. The area removed should be a rough square, approximately 1/8th inch (3mm) on a side just below the point indicated by the pencil tip in the photograph of the bottom PCB surface. Apply electronic grade solder flux if you have it to the newly exposed copper surface and tin.





If you build with this option, extend the T1-D lead slightly and bend it against the tinned square. Solder both the normal pad and the tinned square. If you wish, as an option, the same modification may be made to the top board foil, although it is not necessary.



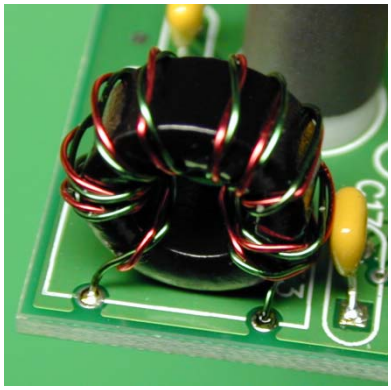
The benefit obtained from this modification is to reduce the ground side track length and unwanted coupling to other signals.

Note that after this modification is made, only one input at J1 is active, as illustrated at the left.

Should it be desired to operate with balanced input at a later date, this modification may be reversed if it is carefully made during installation.

❑ Repeat the process for T3 and install. (There is no option for T3.)

Your transformers should resemble the one photographed at the right.

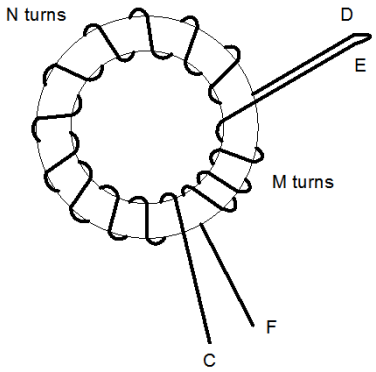


❑ The remaining step is to wind T2 and T4, the matching and feedback transformers. These transformers should be as identical as possible and must be phased (wound) as described below or else you will build an oscillator instead of an amplifier. If you carefully follow the instructions in this manual, your transformers will work the first time. Before winding T2 and T4, take a moment to read the installation steps and study the drawing and photographs.

This manual describes transformers resulting in 11 dB nominal gain, with a 1:11:4 winding ratio. Other winding ratios are possible with different gain as described elsewhere in this manual. In the context of drawing below, this configuration is N=11, M=4.

❑ Cut two lengths of #24 AWG magnet wire, each length 16 inches (400 mm) long.

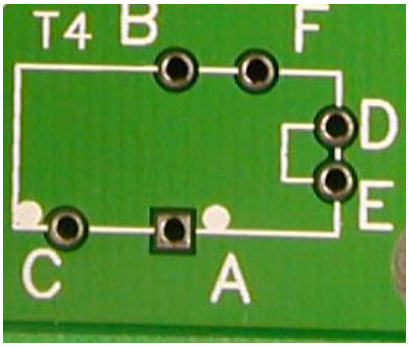
This wire will be wound 15 turns on a ferrite core, as illustrated at the right. The letters C…F on the drawing correspond to T2 and T4's PCB pads. Before winding the transformers, take a moment and look at the PCB outline for T2 and T4.



Start by threading the wire through the core with approximately one inch (25 mm) projecting from the core. This short starting end is C in the drawing.



Wind 11 turns (N) following the orientation shown in the drawing. Note the direction of winding. (I'm left handed and this is how I wind a toroid. And, more importantly, the sense of winding A-B, which is defined by the PCB layout, is based upon following the winding direction illustrated in the drawing.) When completed with all 15 turns, the winding will occupy 80 to 85% of the core perimeter.

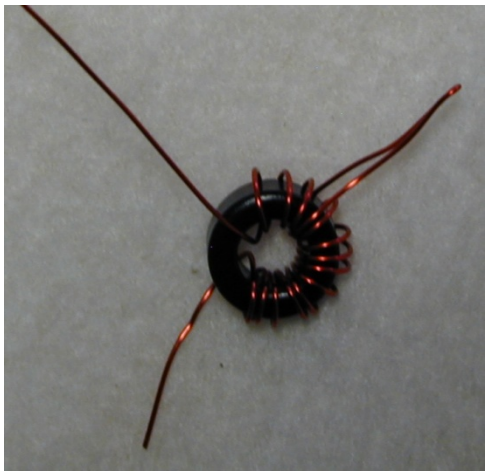


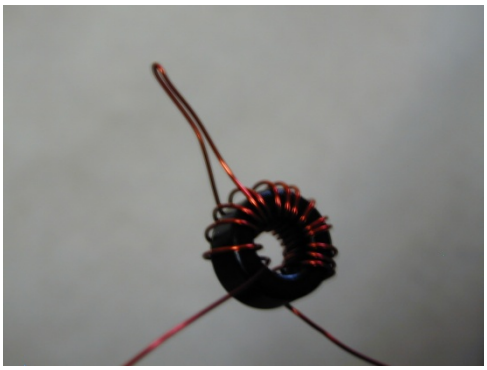
As a reminder, a turn is counted when the wire passes through the hole in the core.

Extend the 11th turn approximately one inch (25 mm)

and double it back. (The doubled wire will become ends D and E). Wind four more turns (M), ending at end F. Trim the F wire to be approximately one inch (25 mm) long.

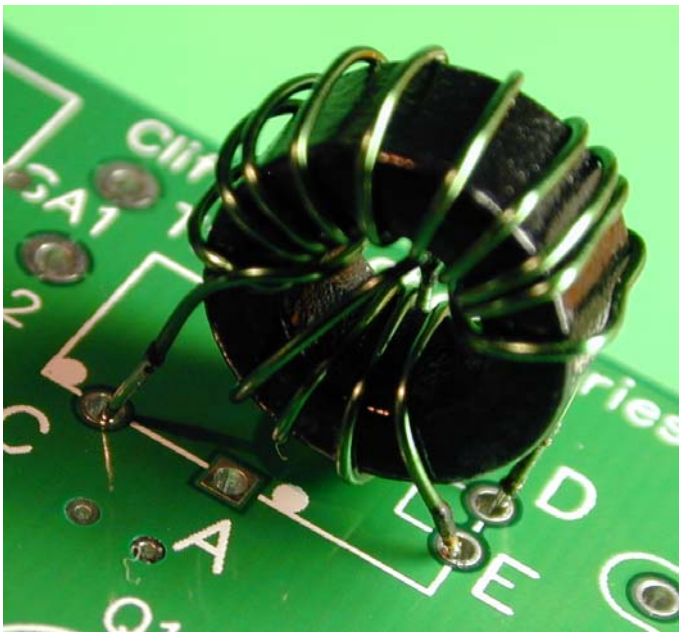
The photos below shows a transformer at this stage, before the loop is cut and the end wires trimmed.



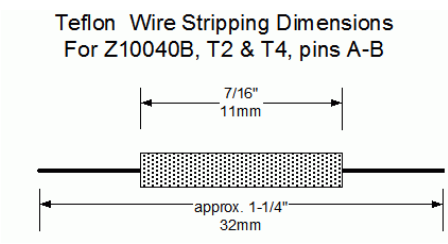


❑ Cut the loop so that the two free ends are approximately one inch (25 mm) long. Remove the insulation on all four ends and tin. You may find it helpful to fit the transformer into the PCB to see how it fits before continuing to the next step.

❑ Insert the leads into T2 holes C, D, E and F, following the drawing, and solder these four leads.



❑ Locate the short length of Teflon insulated wire and cut it into two lengths and remove the insulation as shown in the drawing. These will be the one turn input winding between pads A and B.

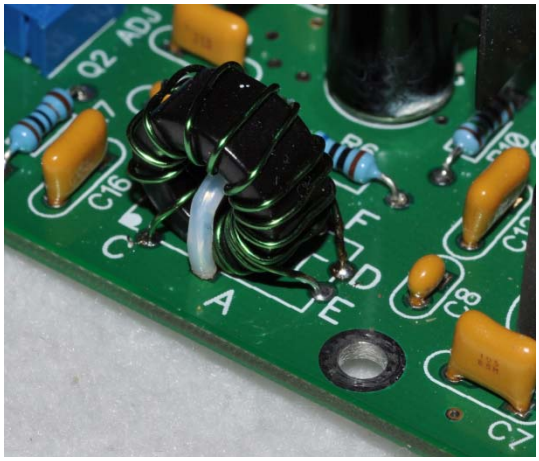


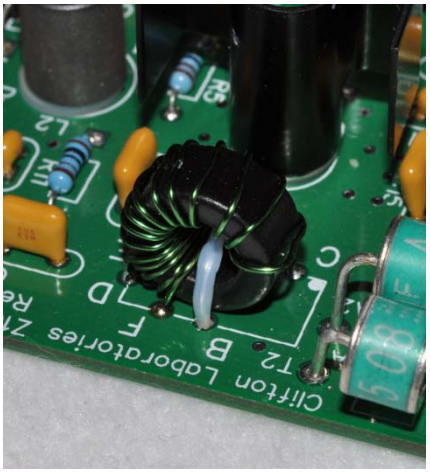
Route the wire through T2's center opening and to pads A and B as shown in the photographs below. You may find it easier to form the wire into a "U" form

before installing it. When properly installed, the Teflon wire will hold the transformer core in place mechanically against the PCB.

❑ Repeat this process for T4 with the second transformer.

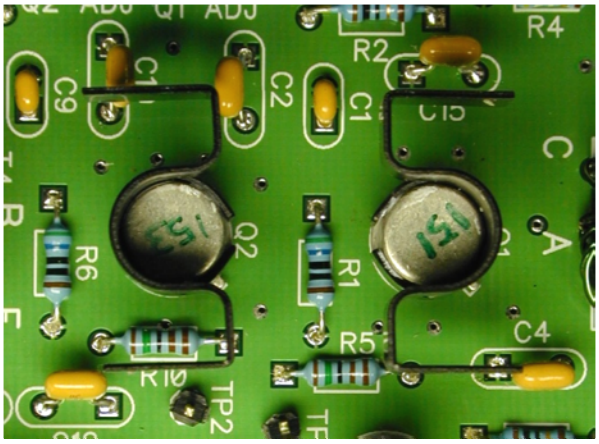
The photographs below show T2 and T4 installed. (Later photographs in this manual show an earlier installation technique that did not use Teflon wire.)





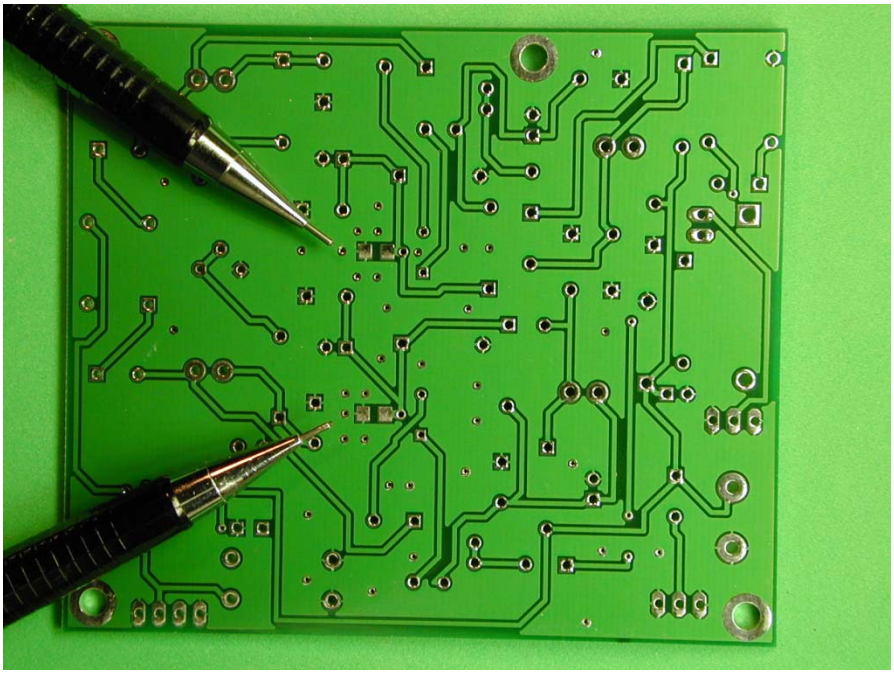
❑ Install the heat sinks on Q1 and Q2. If you have it, a small amount of heat sink compound or thermal grease can be used to improve the thermal connectivity between the heat sink and the transistor body.


In order to provide maximum stability, orient the heat sinks so as to minimize capacitive coupling between Q1 and Q2, following the photograph at the right.



Now install C20 and C21, the 100pF 1206 surface mount capacitors. Both C20 and C21 are mounted on the bottom of the PCB. After installing C20 and C21, please handle the PCB with care to avoid damage to it. DO NOT FLEX the PCB as you may easily crack C20 or C21.

Flip the PCB so that the trace side is up. The pencil tips shows where C20 and C21 are installed.



❑ Installation procedure:

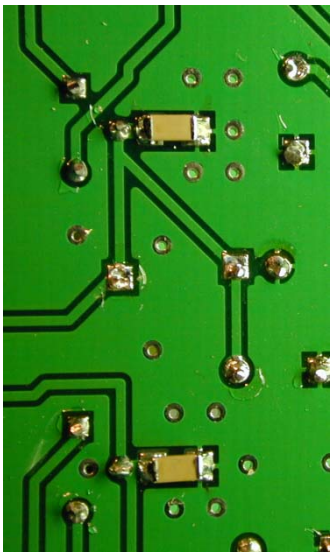
1. Lightly tin the non-ground pads for C21 and C21.

2. Using forceps or a very light touch with long nose pliers, slide C20 into place while heating C20's non-ground pad. Check that C20 is more or less centered on the pads and remove the soldering iron when centered. Too much pressure will crack these parts so use a light touch.

3. Solder the ground pad. Touch up the non-ground pad.

4. Repeat steps 2 and 3 for C21.

5. Although the ground pad uses "thermal relief" it may still be difficult to make with a small soldering pencil, as the large foil area requires more heat capacity than a normal floating pad.

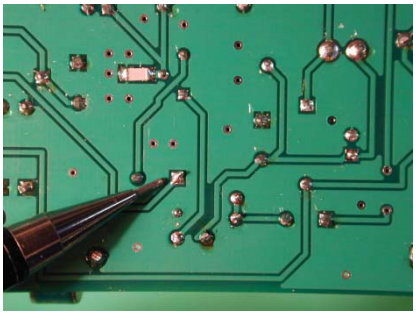


The last components to be installed are 10pF disc ceramic capacitors, C22 and C23. These parts roll off the gain by adding capacitors at VHF/UHF frequencies to improve amplifier stability for 2N5109 transistors exhibiting unusually high UHF gain. This small capacitance does not alter performance within the Z10040B's normal operating range, but it is sufficient to provide stability with the highest gain 2N5109 transistors available to me (beta > 170.)

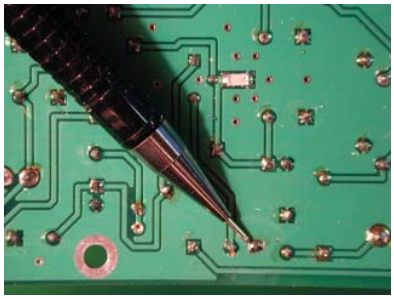
Install C23 between T2-pin A and ground. Trim the leads on C23 to approximately 1/8 inch (3 mm) and tin. On the bottom of the board, locate T2, pin A. Note there is a "solder via" near T2-A as seen in the photo. Tin the via. (Vias are direct connections to the ground

foil and a larger soldering iron than used for normal PCB assembly may be necessary to tin the via.) Orient C23 as illustrated in the photograph and solder it to T2-A and the ground via. After soldering, use an ohmmeter to check T2-A for an inadvertent short to ground. The resistance should be in the 40 – 100 ohm range, depending R2's setting.





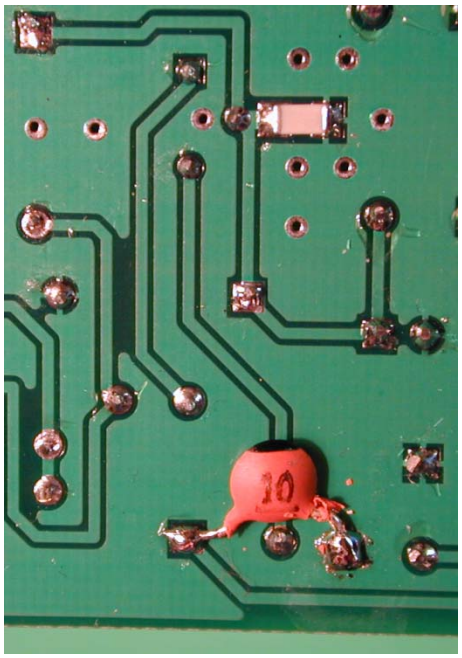
Install C22 between T4-pin A and ground. Unfortunately, there is no convenient ground via, so carefully remove a small area of the solder mask as seen in the photograph at the right. The pencil tip shows the area where the solder mask must be removed.



The solder mask may be removed by gently scraping it away with a sharp hobby knife. The area removed should be a rough square, approximately 1/8th inch (3mm) on a side. Apply electronic grade solder flux if you have it to the newly exposed copper surface and tin it.

Trim the leads on C22 to approximately 1/8 inch (3 mm) and tin. Form the leads as seen in the photograph and solder C22 between T4-A and the new ground point.

After soldering, use an ohmmeter to check T2-A for an inadvertent short to ground. The resistance should be in the 40 – 100 ohm range, depending R8's setting.



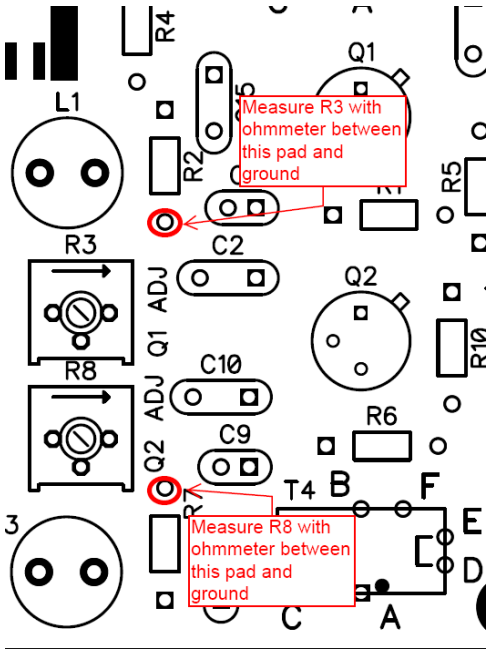
Post Construction Adjustment and Checkout

Before powering up the Z10040B, take a moment to make resistance checks and pre-set R3 and R8.

❑ With an ohmmeter measure and adjust R3 and R8 to 50 ± 2 ohms. (Both measuring points are with respect to ground, with the negative lead of the ohmmeter to ground.)

R3: Measuring point is junction of R3 and R2, as illustrated to the right.

R8: Measuring point is junction of R8 and R7 as illustrated to the right.



You may wish to make a complete set of resistance measurements as developed in the maintenance section of this manual, or you may wish to make an abbreviated set of resistance measurements described below before apply power for the first time.

All readings are taken with a Fluke 189 digital multimeter with low-voltage ohms. Negative lead to ground and positive lead to the indicated test point. Look for gross divergence from these values, not small differences, as different ohmmeters may yield different results where semiconductor junctions are in the path. Since the Z10040B has two identical sections comprising the push-pull design, look for differences in symmetry, where the equivalent point reads significantly different in one section compared with the other.

❑

Abbreviated Resistance Checks Before Applying Power		
Test Point	**Value (Ohms)**	**Comment**
TP1	510	
TP2	510	
Q1 collector	520	Q1's case is internally connected to the collector.
Q2 collector	520	Q2's case is internally connected to the collector.
DC Input (J3) center	510	Should be the same with and without a jumper at J4

❑ If you have not already done so, make up a power cable using a three-pin male header pin. Positive to the center pin and negative to the two outside pins.

❑ The Z10040B will work with DC supply voltages up to 15V and down to 12V. Performance data is based upon 13.8V DC and in general slightly improved intermodulation performance will be seen with supply voltages between 13.8 and 15.0V.



If a laboratory power supply with current limiting is available, set it for a maximum short circuit current of 175 mA and set the voltage to 0V. Connect the supply to the Z10040B at J3 (J4 duplex jumper open) and bring up the voltage slowly whilst observing the current. With R3 and R8 set for 50 ohms, the maximum current observed should be approximately 100 mA at 13.8V. If significant deviations from this value are observed, immediately remove power and investigate.

Adjusting R3 and R8. With the normal DC supply voltage applied through J3 (J4 duplex jumper open) preferably with a laboratory power supply with current limiting set to 175 mA, adjust R3 and R8.



Note: If you adjust R3 or R8 to the zero ohms extreme, it may be possible to damage components in the Z10040B. Some current limiting is built into the circuit, via R2 and R7, together with the resistance of L1 and L3. However, in order to provide the maximum adjustment range to compensate for variations in Q1 and Q2, complete protection against mis-adjustment is not possible. Accordingly, when adjusting R3 and/or R8, it is imperative that you observe the total current being drawn by the amplifier, and, if possible, use a power supply with current limiting set to 175 mA.

In particular, the 1mH shielded inductors used at L1, L2, L3 and L4 are rated for a maximum DC current of 90 mA. Under no circumstances should Q1 or Q2 be biased to draw more than 75 mA each.

❑ Alternative 1: If you do not have the ability to measure 3rd order and 2nd order intermodulation products, adjust R3 and R8 such that Q1 and Q2 have substantially equal collector currents of approximately 45 mA each.

Collector current is determined by measuring the voltage drop across the 10R0 resistors, R11 and R9 via TP1 and TP2. The drop across R9 and R11 represents the sum of the collector current and the current drawn by the base bias network, which is approximately 6 mA.

Connect a DC voltmeter between the junction of F1/RV1 (positive lead) and TP1 (negative lead.) Adjust R3 until the voltmeter reads 0.500 ±0.050 volts. This corresponds to 50 mA total current, consisting of approximately 44 mA collector current through Q1 and 6 mA bias network current. Record the DC voltage: _____

Move the negative lead to TP2 and adjust R8 for the same reading recorded above. This will set Q2's collector current to approximately match Q1's current.

❑ Alternative 2: Adjust R3 and R8 for best 3rd and 2nd order intermodulation performance using the test equipment configuration you normally use for these measurements. During the adjustment process do not exceed 75 mA in either Q1 or Q2 as it is possible to damage components with over-current.

A bias adjustment service for kit builders not equipped to measure IP2 and IP3 is available. Contact Clifton Laboratories for details.

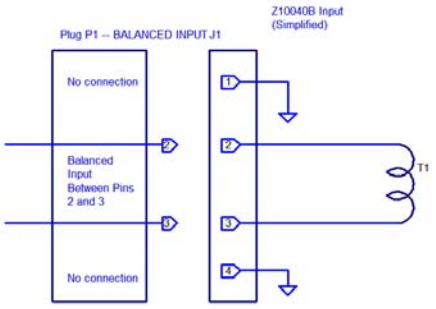
Input and Output Connections

Output and DC power connections are made to the Z10040B with 3-pin headers. Since the outside pins are always ground, either orientation is permitted. Input to the Z10040B is made with a 4-pin header and may be configured for either balanced or unbalanced input.

Balanced Input

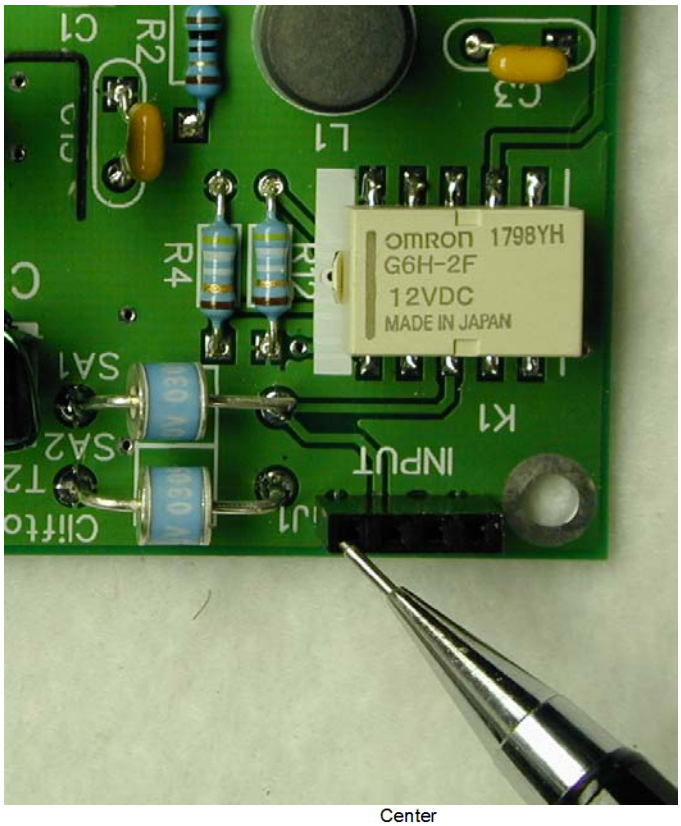
To make a balanced connection to the Z10040B, use J1's two center pins, as illustrated in the drawing to the right.

If a shielded pair is used for the balanced input, the shield should be connected to the two outside pins, which are common with the Z10040B's ground plane.



Unbalanced Input

An unbalanced input to the Z10040B should be made as described. The described method is necessary for improved stability.



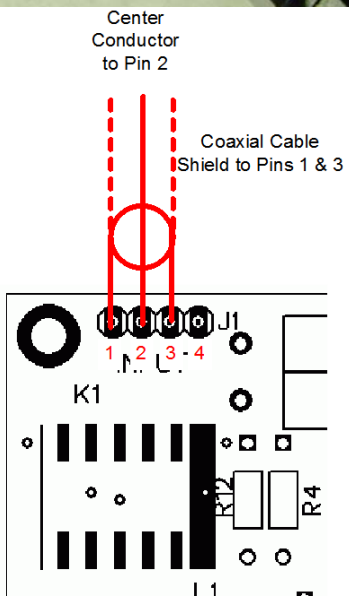
The pencil point in the photo identifies J1, pin 4.

When using unbalanced input, connect the coaxial cable so that the center conductor mates with pin 2 and the shield connects to pins 1 and 3. Pin 4 may be left unconnected.

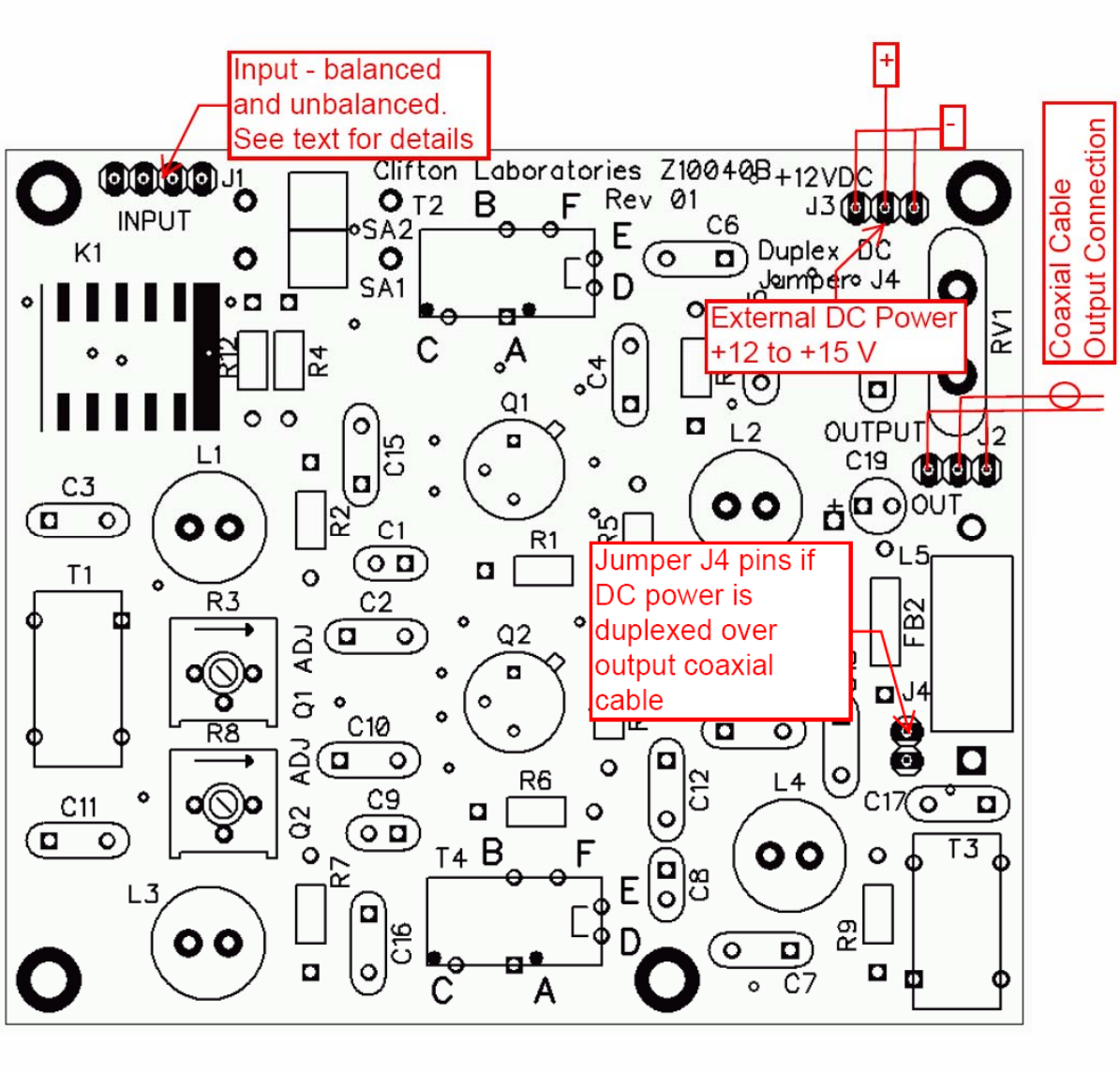
<u>Do not use a connection that places the shield on J1, pin 2 and the center conductor on J1, pin 3</u>.

As always when making connections to a high gain amplifier, shielded coaxial cable should be used on the output (and the input if unbalanced) and the output cable should not be routed near the input. If balanced input is used, the input cable should be twisted pair or shielded pair to avoid unwanted signal pickup or feedback and oscillation.

Note: If the unbalanced-only modification is made, as described earlier in this manual, only the input connection illustrated to the right will function.



Connections Diagram



This completes the assembly and verification of your Z10040B Norton Amplifier.

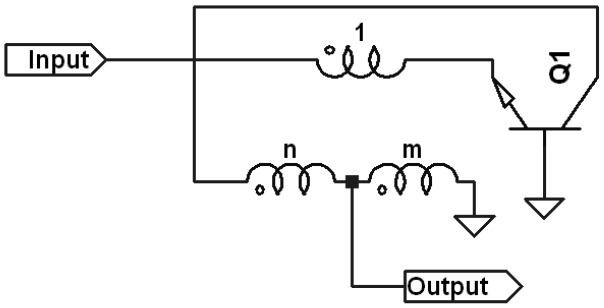
Schematic and Theory of Operation

Theory of Operation

The Z10040B Norton amplifier consists of two identical amplifier sections arranged in push-pull.

The discussion below uses component designations for the section associated with Q1.

Each section is a common base (also known as "grounded base") amplifier. As such, essentially identical signal currents flow through all three sections of T2 and T1's secondary winding. Gain is achieved in the grounded base amplifier because the collector load, represented by T2's n and m windings operating as an auto-transformer has greater impedance than the emitter input, and hence power gain results.



The figure at the right is a simplified view of an amplifier section, with all DC biasing and blocking components removed so that we may concentrate on the signal flow. The transformer turns ratios are shown as 1:n:m, but this does not mean the emitter feedback winding must have only one turn. Rather, it is the ratio of turns that is important, so that if the emitter winding has, for example, two turns, then the number of turns in windings n and m should also be doubled.

Consider windings n and m and assume a load of impedance Z is connected from output to ground. Windings n and m form an auto-transformer with Q1's collector seeing an impedance of:

$$Z_C = Z_O\left(\frac{n+m}{m}\right)^2$$

Since the same signal current flows through the emitter and collector (neglecting base current), the gain of the common base amplifier is proportional Zc or n and m in this relationship.

The transformer turns ratios should not be arbitrarily selected, if the full benefits of the Norton amplifier are to be realized. From Patent No. 3,891,934, the following equation governs the transformer turns relationship:

$$n = m^2\left(\frac{R_S}{R_L}\right) - m - 1$$

$$n = m^2 \left(\frac{R_S}{R_L}\right) - m - 1$$

Where

R_S is the source (input) impedance

R_L is the load (output) impedance

n and m are the transformer winding ratios, normalized to an emitter winding with one turn.

In our case, we wish the input and output impedances to be equal, and hence $R_S/R_L = 1$. Thus the turns relationship is simplified to:

$n = m^2\text{-}m\text{-}1$

The amplifier's transducer gain[1] is stated as:

$$G_t = m^2 \frac{R_S}{R_L}$$

Again, since our normal operation is with equal input and output impedances, the transducer gain G_t is simply m^2.

Winding Ratio 1:n:m	Transducer Gain (dB)
1:1:2	6.0
1:5:3	9.5
1:11:4	12.0
1:19:5	14.0
1:29:6	15.6

These figures are theoretical and the actual realizable gain is typically a dB or so less. See Appendix F for measured data on a 1:29:6 amplifier.

One significant advantage of the Norton amplifier is that the input impedance automatically tracks the output impedance. Thus, if terminated into a 50 ohm load, the input impedance is 50 ohms. If the output impedance is changed to 75 ohms, the input impedance becomes 75 ohms. (This relationship is again not perfect, but it is reasonably good with less than a 2:1 VSWR over the range 300 KHz – 30 MHz when measured in a 50 ohm system.)

DC power may be provided to the Z10040B via two feed points. First, a three-pin connector permits direct DC power connection. Secondly, adding a jumper at connector J4 permits DC power to be duplex fed over the coaxial cable transmission line carrying the amplifier's output. Of course, an

1 Transducer gain is defined as: "the ratio of the power delivered by a network to a load (PdL) to the power available from the source (Pas). Transducer gain is a function of the source and load reflection coefficients and the network s-parameters." http://www.maurymw.com/support/faqs/faqs/faq9.html

appropriate DC power injector, such as Clifton Laboratories model Z1203A, will be required and the power source that is used should be selected to have low noise at the frequencies of interest.

Over current protection is provided by F1, a 200 mA positive temperature coefficient "polyfuse." Should the amplifier draw more than 200 mA, F1 will heat and switch to a high resistance state, thereby limiting the current drawn by the power source. So long as the voltage remains applied, F1 will remain in the high resistance state.

Over voltage protection is provided by RV1, an 18V DC (nominal) bipolar metal oxide varistor. The primary purpose of RV1 is to limit damage to the DC power source, should a nearby lightning strike or other incident induce a greater than normal voltage on the DC power line. Although RV1 is rated to begin clamping at 18V (1.0 mA clamp current at 18V), the actual onset voltage may be 20% above this figure and the clamping voltage may rise as high as 36V at 50A clamping current. Hence, even with RV1 in place and functioning properly, excessive over voltage may still occur if the disturbing event is sufficiently energetic. (The ROV14-180M device used in the Z10040B is rated at a one-time 1,000A clamp or two-times 500A clamp. However, at 1000A, the expected clamping voltage is 80V.)

Reverse voltage protection is provided by D1, a 1N400x series diode connected to be forward biased if the input polarity reverses. This causes two things to happen. First, the maximum voltage across the DC power distribution circuitry will be limited to approximately 1V by D1. Secondly, fuse F1 will enter into high resistance mode by virtue of the over current. Of course, a sufficiently robust power supply connected with reverse polarity may destroy D1 before F1 can enter high resistance mode.

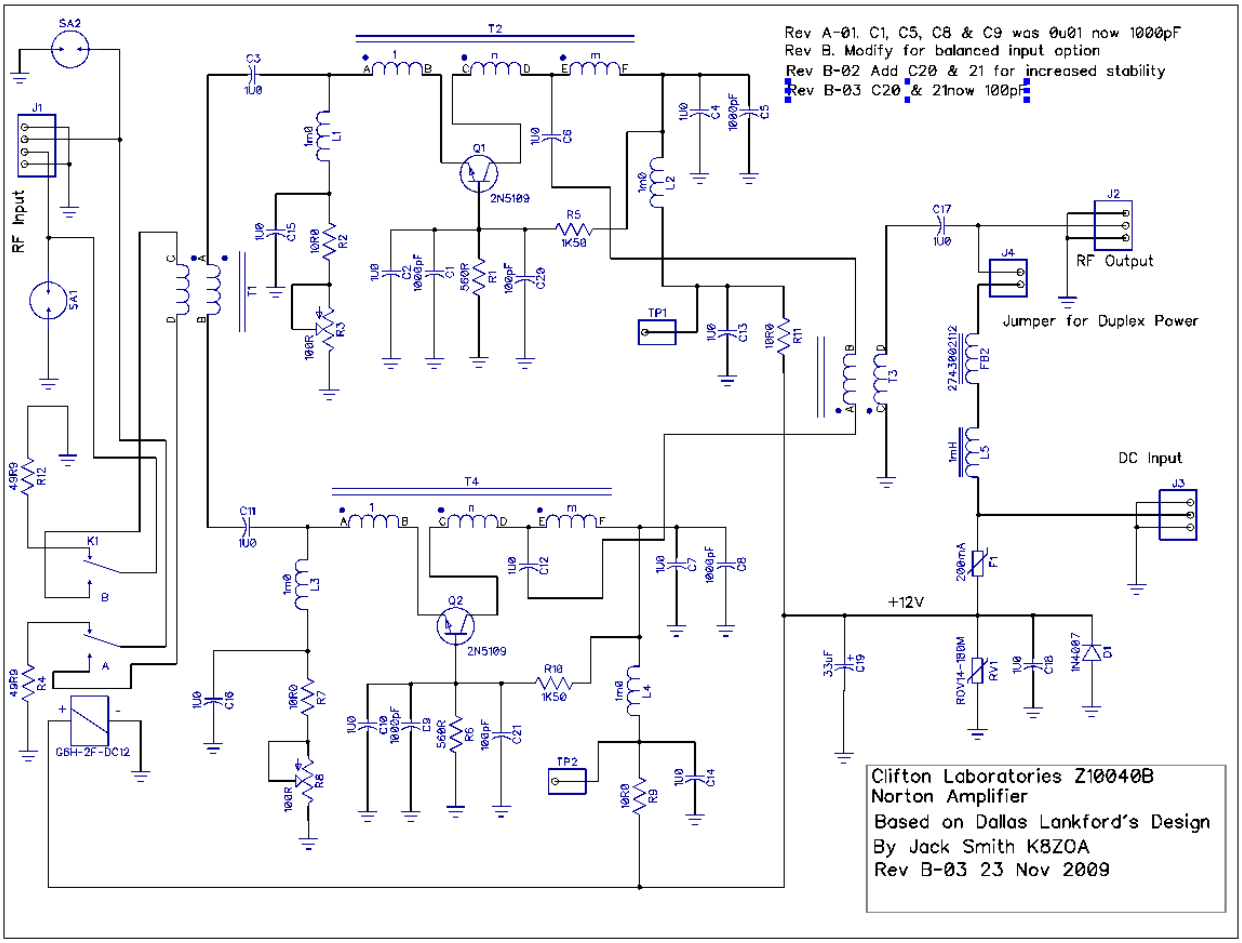
The Z10040B's input is through a bifilar wound, broadband transformer, T1. Both of T1's primary terminals are brought out to J1 through K1's contacts so that either balanced or unbalanced input may be used. Balanced input signals are applied across T1's primary, which remains floating with respect to ground. If unbalanced input is used, one of T1's primary terminals is connected to ground through appropriate jumper settings at J1, or via the ground connection modification discussed in the assembly section of this manual.

The Z10040B's input circuit is protected in two ways. First, when DC power is removed from the Z10040B, relay K1 removes the input connection and connects it to ground through R4 and R12, 49R9 ohm resistors. (If desired, the user may replace R4 and R12 with wire jumpers to the input when power is removed.) Secondly, SA1 and SA2, "gas trap" or spark protector devices are always connected across the Z10040B's input connector. Although SA1 and SA2 limit the voltage for fast rise time pulses, their break over voltage may be several hundred volts. The primary purpose of SA1 and SA2 is to limit the voltage that might otherwise be coupled over the coaxial transmission line and, secondarily, to provide some protection to the Z10040's components.

When the input is configured as unbalanced, only one of SA1 and SA2 is operational. In balanced mode, SA1 and SA2 are connected between the two balanced inputs and the Z10040B's common ground point. Likewise in balanced mode, when the Z10040B is unpowered, R4 and R12 are connected across the balanced input to the Z10040B's common ground point.

All of these protection measures assume that the Z10040B is properly grounded and that good engineering practices have been used in its installation and construction of the ground system. The Z10040B is not intended to survive a direct lightning strike to an antenna connected to its input, whether powered up or not. However, the protective measures incorporated into the Z10040B's design should aid in reducing damage, particularly where the strike is not directly to the antenna system.

Schematic[2]

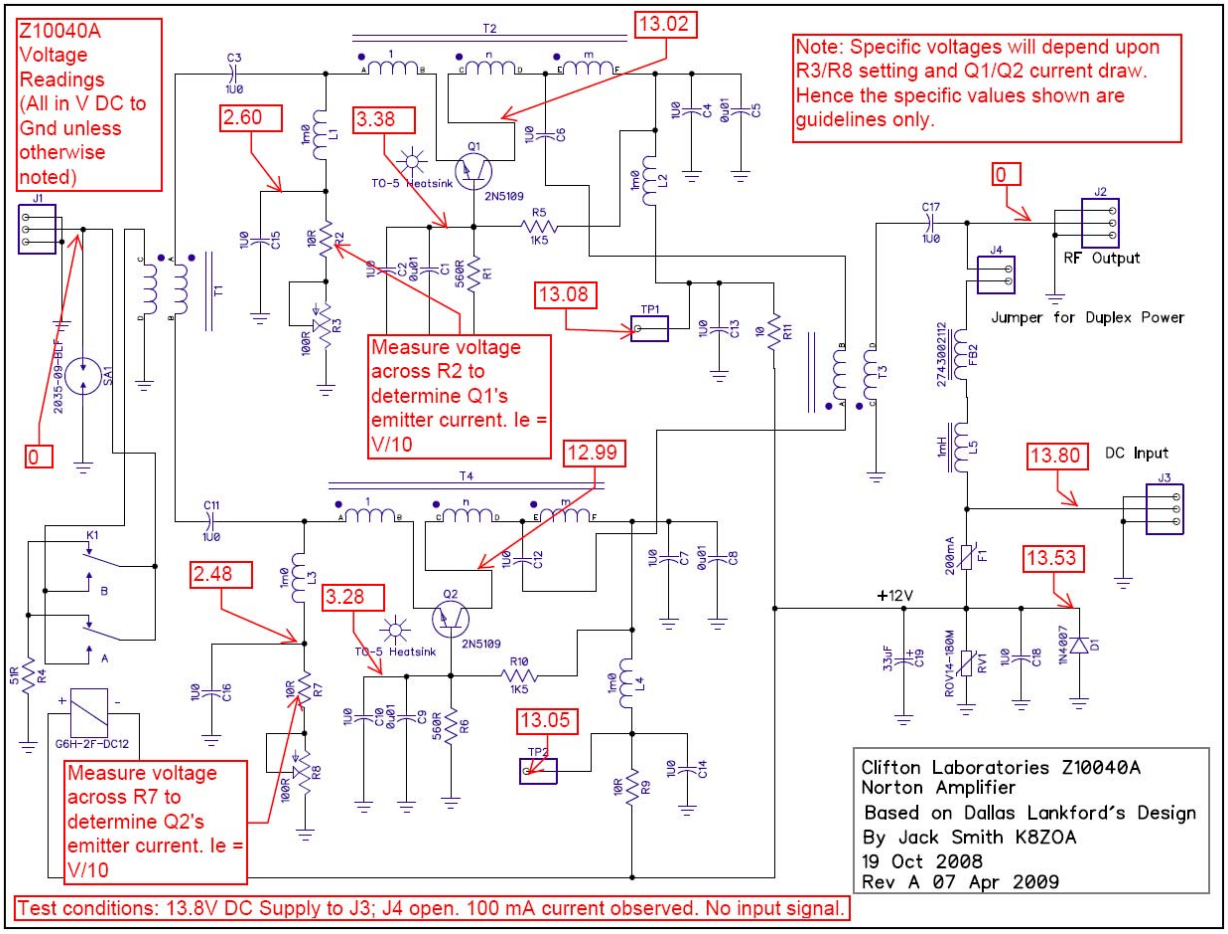


[2] The schematic does not show C22 and C23. See the manual backdating section for C22/C23 connection points.

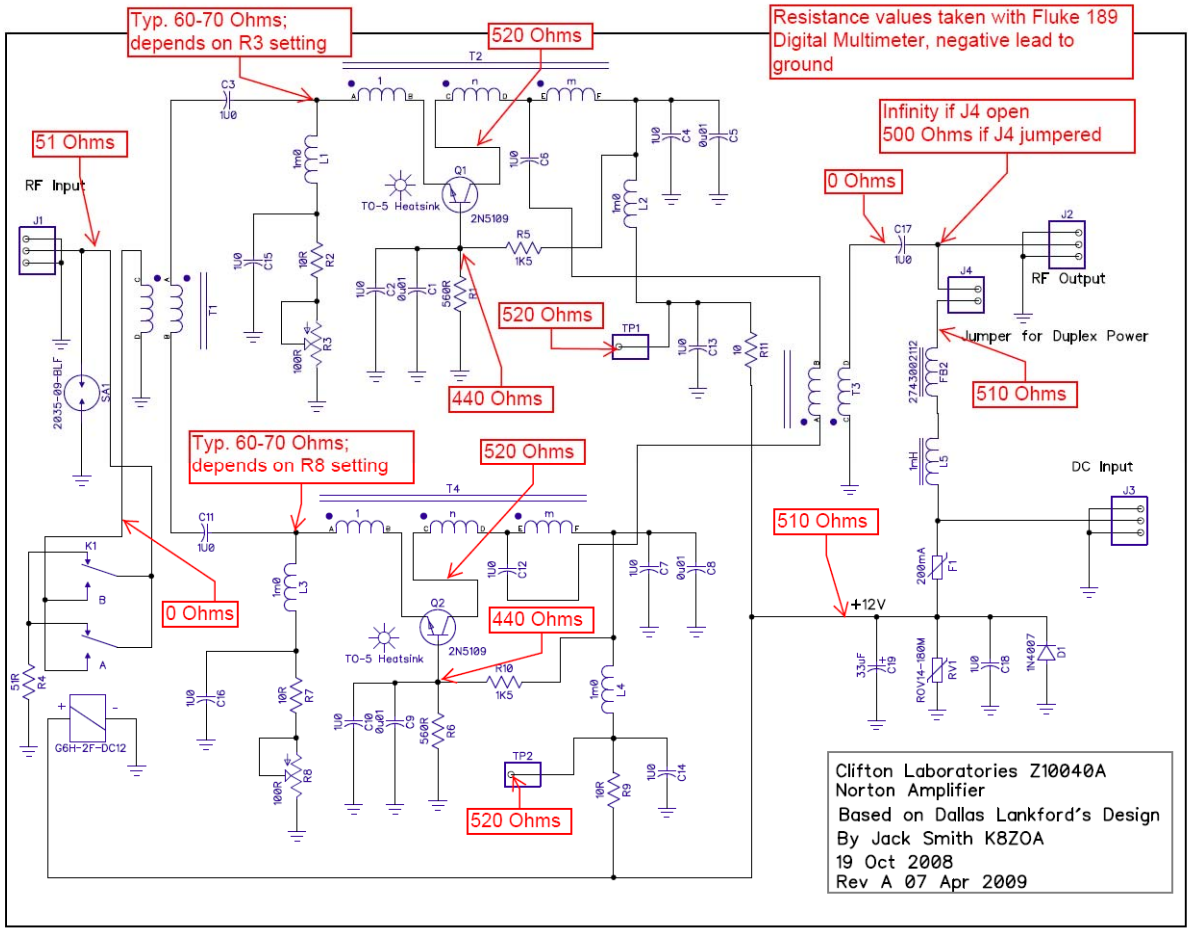
Troubleshooting Guide

The following annotated schematics provide resistance and typical operating voltage data for the Z10040B. (The schematic shown is the Z10040A. No resistance or voltage changes exist between the "A" and "B" versions of the Z10040.)

Voltage Data



Resistance Data



Appendix A Typical Performance Data

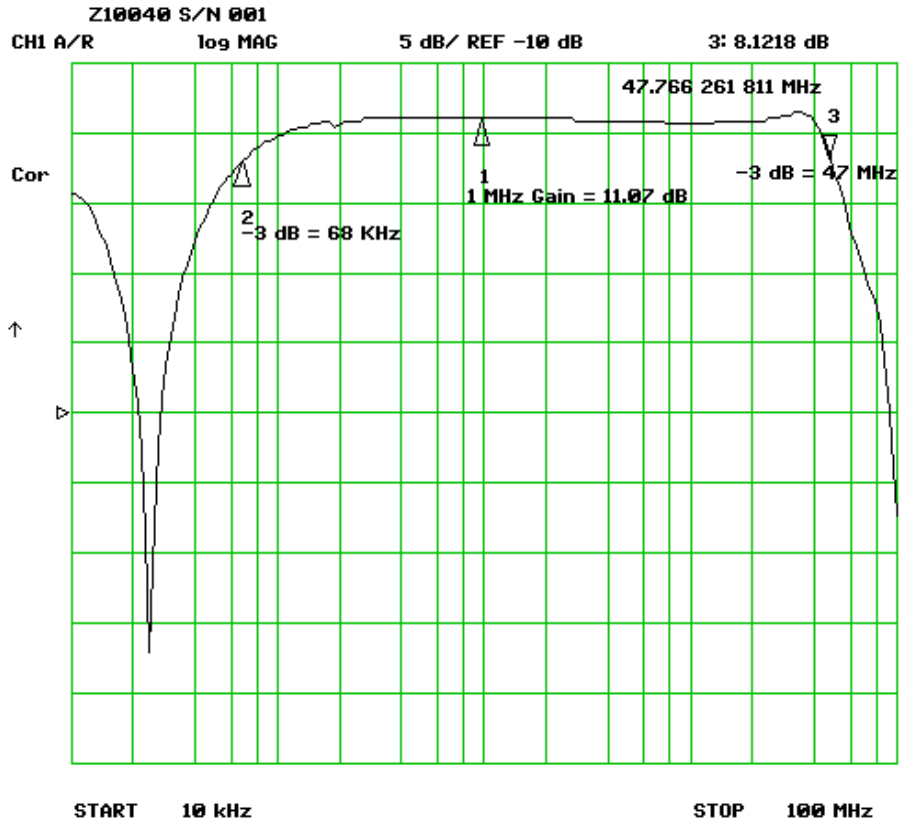
Except for common mode rejection, the data presented below is taken from one Z10040A amplifier. There is no significant performance difference between the “A” and “B” versions of the Z10040, except for differences associated with operating a balanced input.

While it is believed representative of Z10040A and B amplifiers, due to component tolerance, assembly practices and test setup, the performance level seen in these measurements should be regarded as *typical* and is not guaranteed.

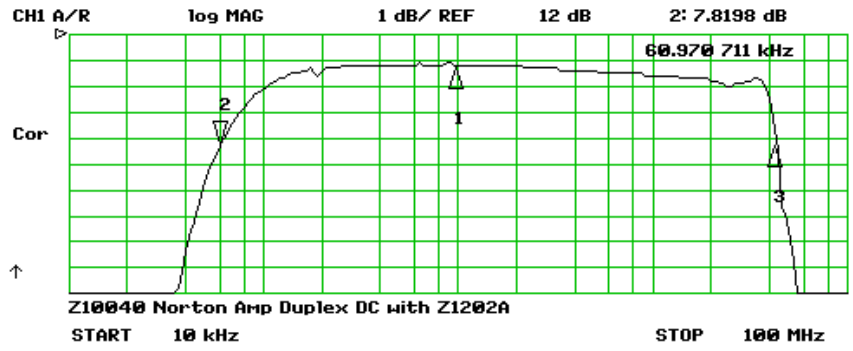
Unless otherwise specifically noted, the data is taken with unbalanced input.

Bandwidth

Test Conditions: Direct DC feed.



Test Conditions: Duplex DC feed over coaxial cable with Clifton Laboratories Z1202A power coupler.



N	STIMULUS	val
1	1 MHz	10.832 dB
2	60.970 711 kHz	7.8198 dB
3	43.064 683 001 MHz	7.8390 dB

Second and Third Order Intermodulation

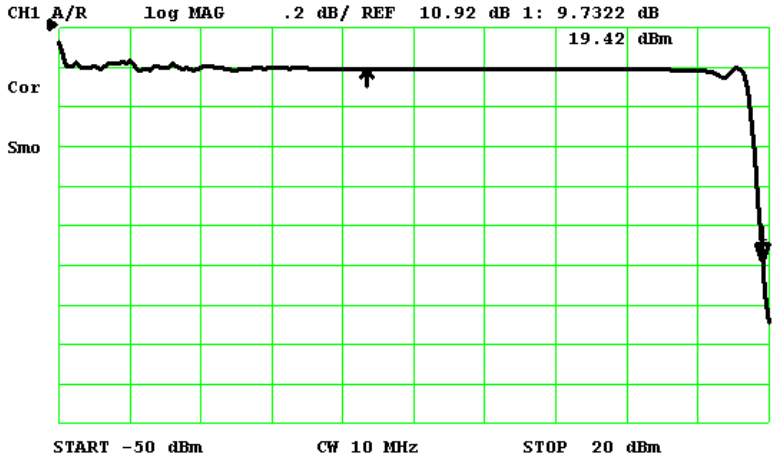
Test conditions: Two test signals at 3007 KHz and 4011 KHz, adjusted to provide an output level of 0 dBm for each tone. The following measurements were made on a typical Z10040B.

Frequency (KHz)	Order	Level (dBm)	Intercept (dBm)(output based)
1004	2nd	-85.1	OIP2: +85
2003	3rd	-93.6	OIP3: +47
5013	3rd	-95.2	OIP3: +47
7018	2nd	-82.2	OIP2: +82

1 dB Gain Compression

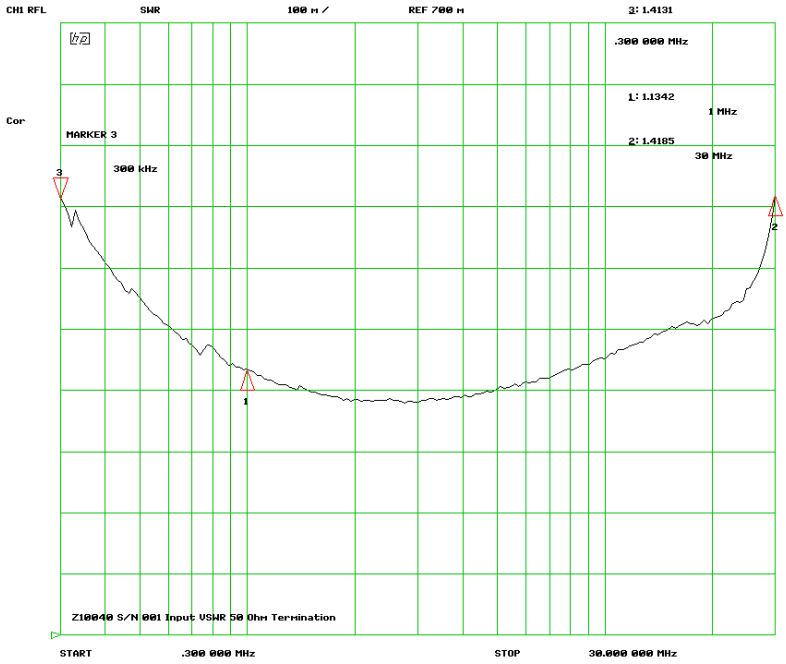
Test Conditions: CW signal at 10 MHz, Z10040 input level between -50 dBm and +20 dBm. 1 dB gain compression point +19.42 dBm input.

Note: This test can easily damage test equipment as the output power approaches 1 watt. Appropriate attenuators must be used to limit signal levels to safe values.



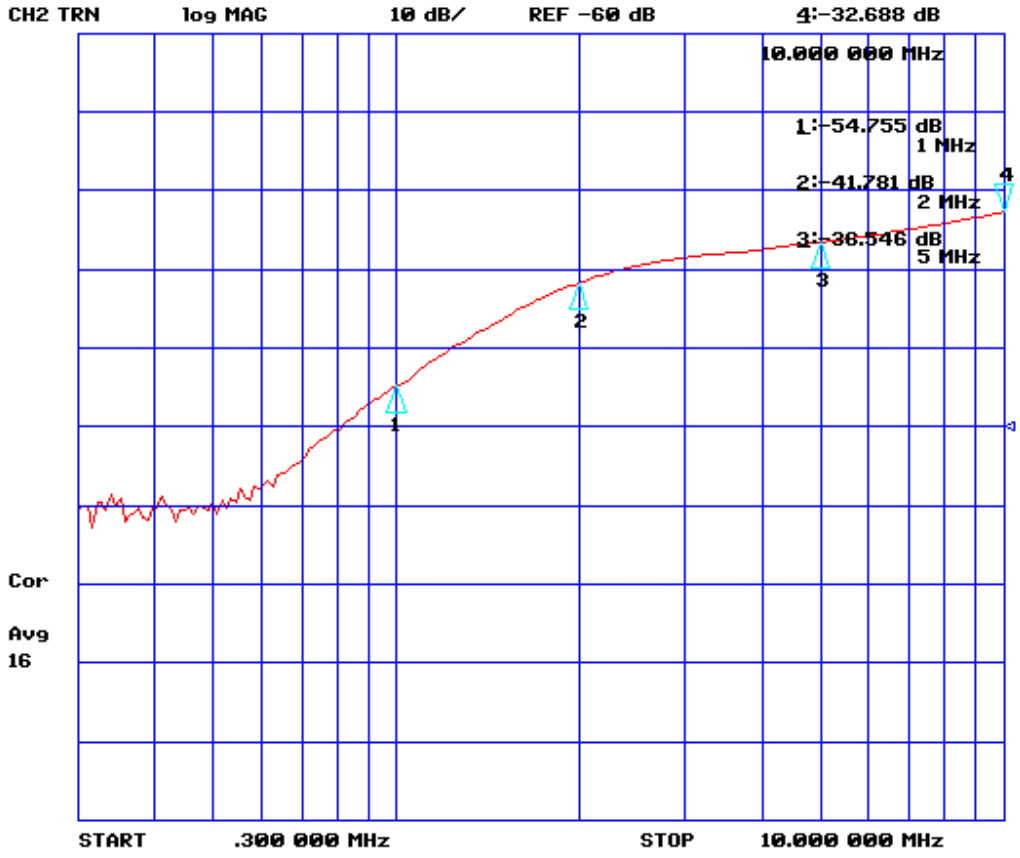
Input VSWR

Test conditions: Terminated with 50 ohm load, 13.8V DC power.



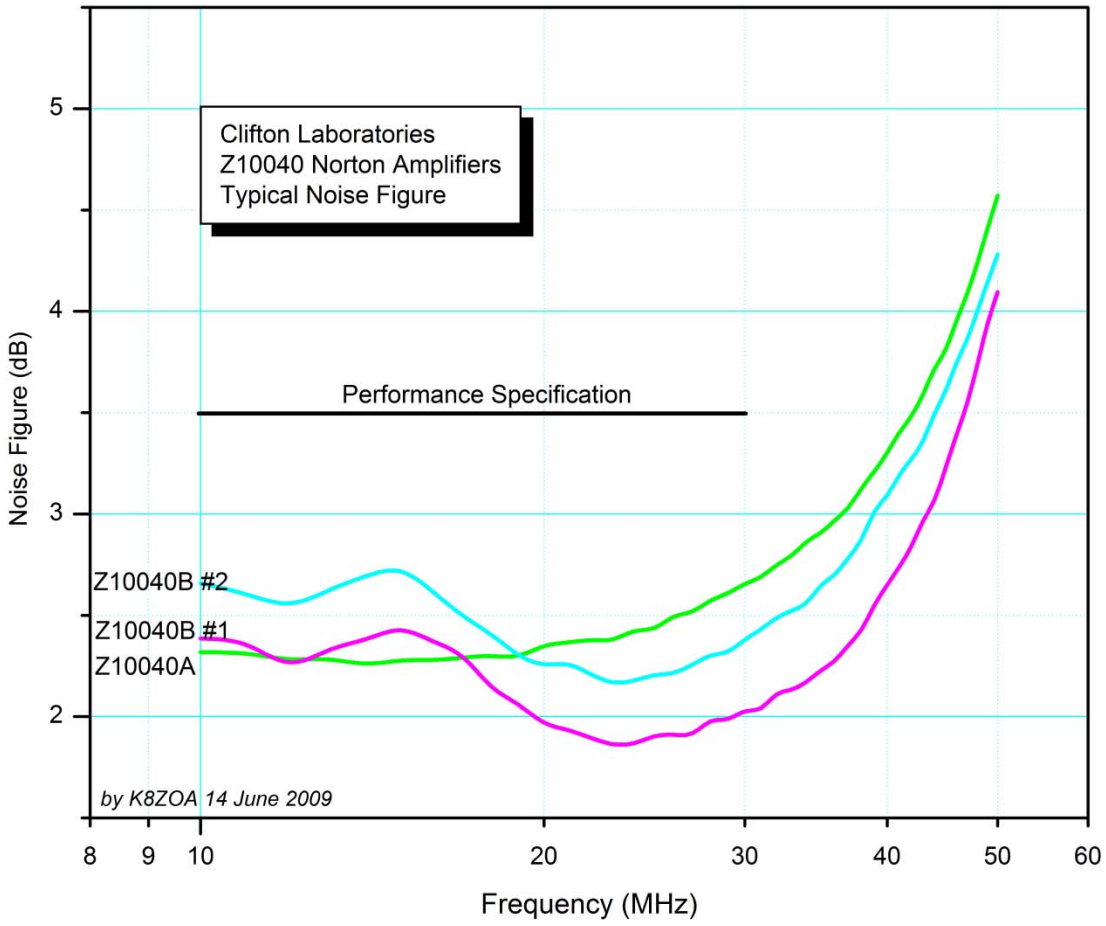
Common Mode Rejection

Test conditions: Unbalanced input applied to J1 pins 2 and 3 in parallel. Ground to J1 pins 1 and 4. Frequency range: 300 KHz – 10 MHz. Input signal level -15 dBm. Plot shows output signal level, with 0 dB being a direct connection between input and output.



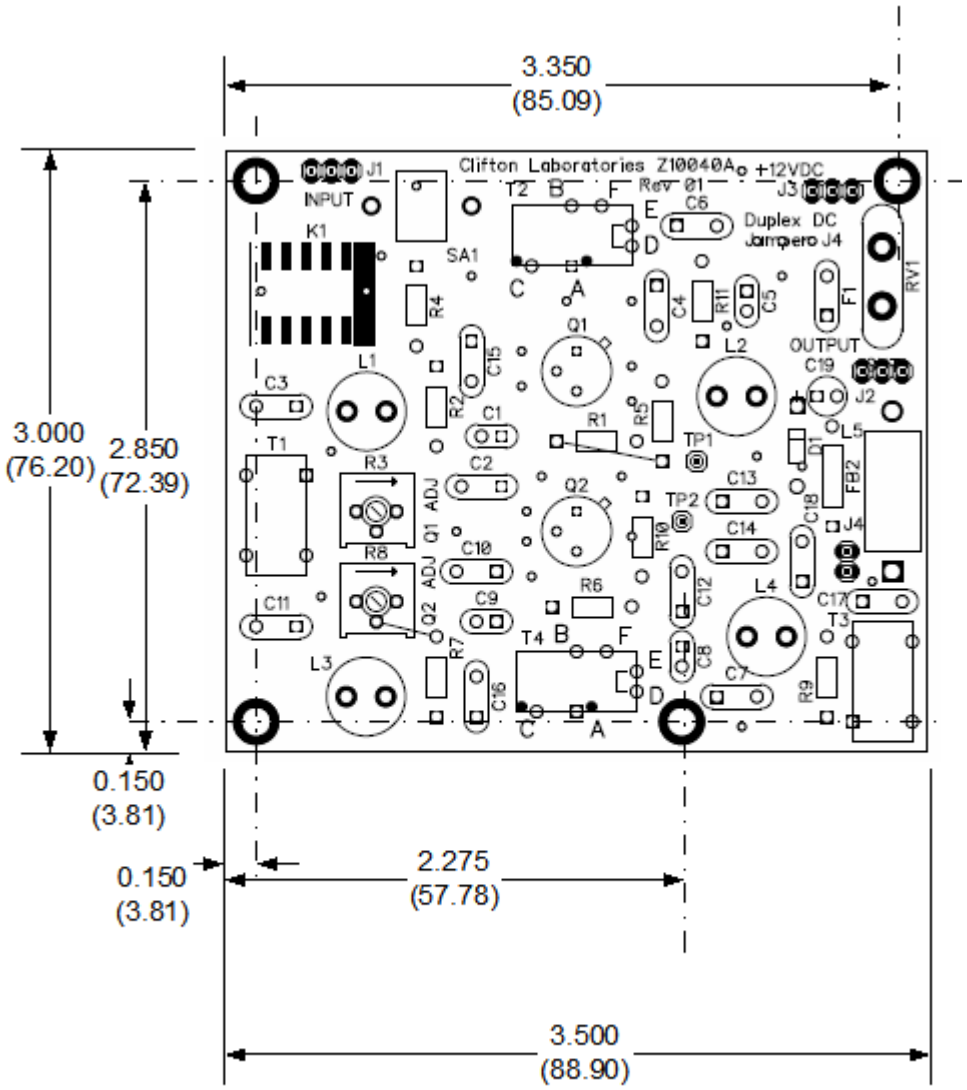
Noise Figure

Data taken with an HP8970A noise figure meter and AIL 7615 noise source at 15V supply. Noise figure differs by as much as 1 dB from amplifier to amplifier.



Appendix B – PCB Mounting Hole Dimensions

Drawing is **not** to scale. There is no change in mounting hole spacing and size between the Z10040A and Z10040B.



Dimensions in inches and (mm)

Appendix C – Norton Amplifier Patent, US Patent No. 3,891,934

United States Patent [19]

Norton et al.

[11] **3,891,934**

[45] **June 24, 1975**

[54] **TRANSISTOR AMPLIFIER WITH IMPEDANCE MATCHING TRANSFORMER**

[75] Inventors: **David E. Norton**, Framingham, Mass.; **Allen F. Podell**, Los Altos, Calif.

[73] Assignee: **Adams-Russell Co., Inc.**, Waltham, Mass.

[22] Filed: **May 22, 1974**

[21] Appl. No.: **472,281**

[52] **U.S. Cl.** **330/21**; 330/19; 330/26; 330/165; 330/188; 330/195

[51] **Int. Cl.** **H03f 3/04**

[58] **Field of Search** 330/12, 19, 21, 22, 40, 330/165, 188, 195

[56] **References Cited**

UNITED STATES PATENTS

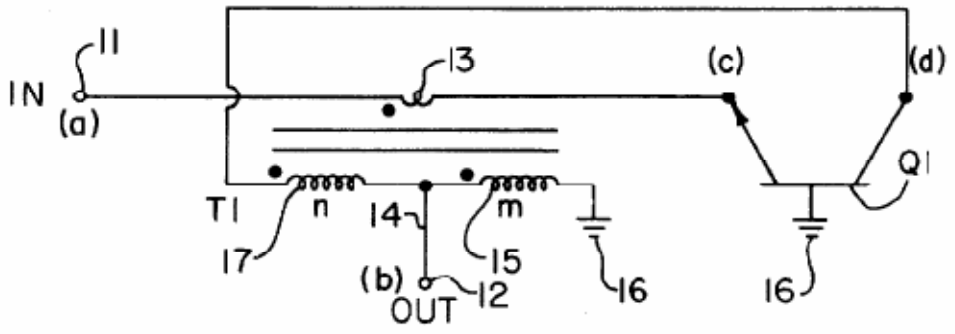
2,691,077	10/1954	Korns	330/40 X
2,701,281	2/1955	DeWhite et al.	330/12 X

Primary Examiner—R. V. Rolinec
Assistant Examiner—Lawrence J. Dahl
Attorney, Agent, or Firm—Charles Hieken, Esq.; Jerry Cohen, Esq.

[57] **ABSTRACT**

An amplifier includes a transistor and transformer having a primary winding and a tapped secondary winding. The primary winding is connected in series between the input terminal and the transistor emitter. The transistor base and one end of the secondary winding is grounded. The other end of the secondary winding is connected to the transistor collector. The transformer secondary tap is connected to an output terminal. The ratio of that portion of the secondary turns connected between the tap and *r-f* ground and the primary turns is m. The ratio of that portion of the secondary turns connected between the tap and the transistor collector and the primary turns is n. For two-way impedance match between a source resistance R_s and a load resistance R_L, $n = m^2 (R_s/R_L) - m - 1$.

8 Claims, 5 Drawing Figures



1

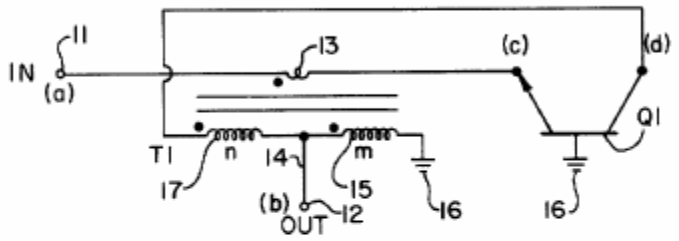


FIG. 1

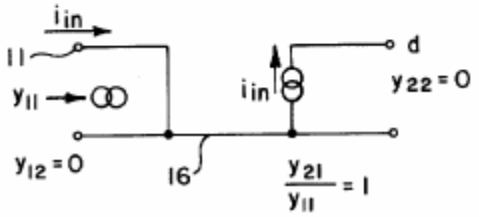


FIG. 2

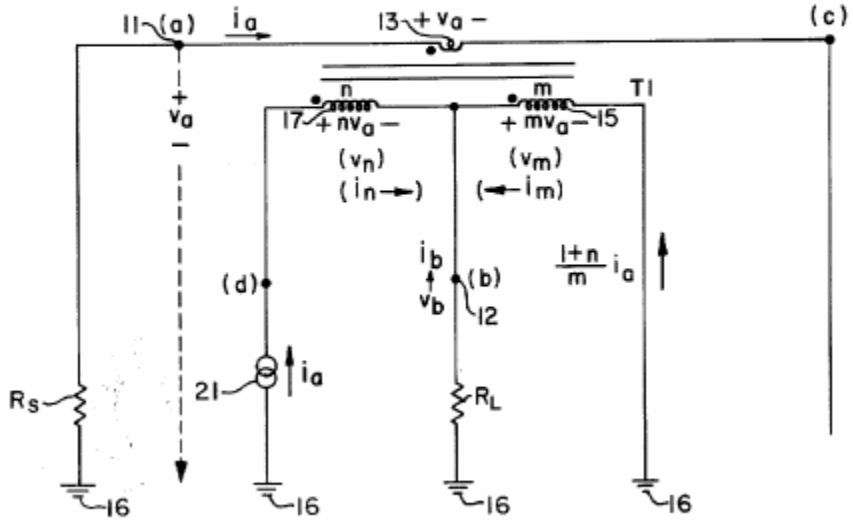


FIG. 3

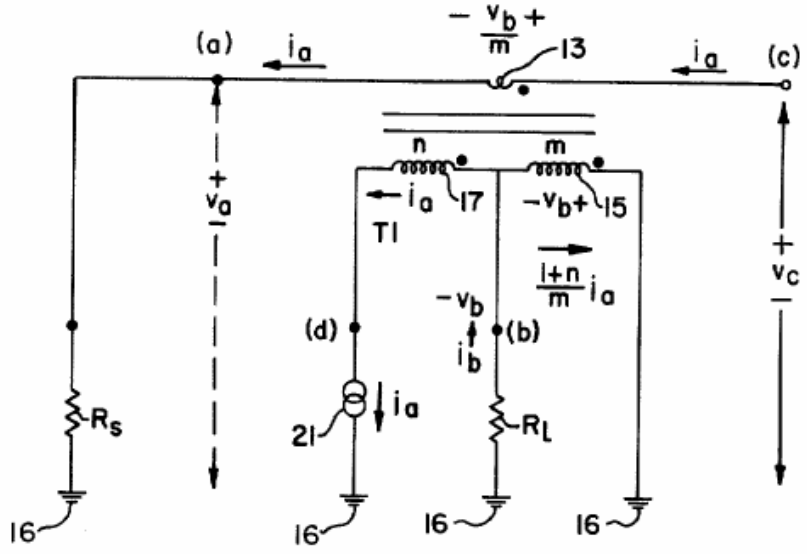

(a)
i_a
$-\frac{v_b}{m}+$
13
i_a
(c)
n
m
$+v_a-$
i_a
17
$-v_b+$
15
T1
$+v_c-$
$\frac{l+n}{m} i_a$
$-v_b$
(d)
(b)
i_b
i_a
21
R_s
R_L
16
16
16
16

FIG. 4

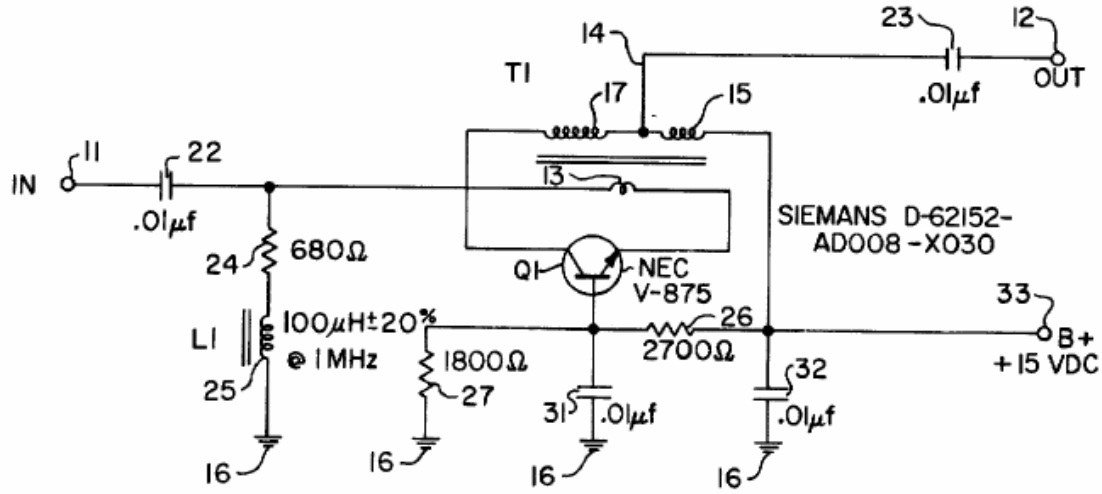

14
23
12
T1
17
15
.01μf
OUT
IN
11
22
13
.01μf
SIEMANS D-62152-
AD008-X030
24
680Ω
Q1
NEC
V-875
33
L1
100μH±20%
@ 1MHz
26
2700Ω
B+
+15 VDC
1800Ω
27
31
.01μf
32
.01μf
25
16
16
16
16

FIG. 5

TRANSISTOR AMPLIFIER WITH IMPEDANCE MATCHING TRANSFORMER

BACKGROUND OF THE INVENTION

The present invention relates in general to ampifying and more particularly concerns a novel amplifier with high dynamic range and efficiency especially useful in matching both a source impedance and a load impedance while providing *r-f* amplification over a relatively broad band with a single transformer and single transistor.

CATV coaxial cable systems that transmit and amplify television signals use many amplifiers representing a significant cost of the system. To avoid reflections that cause undesirable visible ghosts on a television screen, care is taken to properly terminate the transmission lines. Thus, both the input and output of an amplifier should match that of the transmission line to which it is connected. While techniques for achieving this result are known, conventional prior art circuits involve many components that are relatively costly to acheive this result.

Still another problem arises from the range of signal levels to be amplified. It is difficult to amplify low level signals adequately and avoid overloading the amplifier with high level signals. Furthermore, dissipation of *r-f* power in amplifying circuit resistors reduces efficiency.

Accordingly, it is an important object of this invention to provide an economical low-noise *r-f* amplifier with high dynamic range and efficiency capable of conveniently matching both a source impedance and a load impecance while providing good amplification over a relatively broad bandwidth.

It is another object of the invention to achieve the preceding object with relatively few components.

It is a further object of the invention to achieve one or more of the preceding objects with relatively few components, none of which need be adjusted once circuit design is complete.

It is still a further object of the invention to achieve one or more of the preceding objects with a circuit that has only one transistor and one transformer.

SUMMARY OF THE INVENTION

According to the invention, there is an amplifying device having control, input and output electrodes, such as a transistor having at least base, emitter and collector electrodes. Means are provided for effectively connecting at *r-f* the control electrode or base to a common or reference terminal. Transformer means having at least a primary winding and a tapped secondary winding has the primary winding coupled in series between an input terminal and the imput electrode or emitter and its secondary winding effectively coupled between the common terminal and the transistor collector. An output terminal is coupled to a tap between first and second portions of the transformer secondary winding, the first portion being coupled between the tap and the common terminal. The ratio of first portion turns to primary turns is m; of second portion turns to primary turns, n. Preferably $n = m^2(R_s/R_L) - m - 1$ where R_s and R_L are the source and load resistances to be matched at the input and output terminals, respectively.

Numerous other features, objects and advantages of the invention will become apparent from the following specification when read in connection with the accompanying drawing in which:

BRIEF DESCRIPTION OF THE DRAWING

FIG. **1** is a schematic circuit diagram of an embodiment of the invention;

FIG. **2** is a representation of the transistor as an ideal common base circuit with various admittance parameters;

FIG. **3** is an equivalent circuit of the circuit of FIG. **1** helpful in understanding the mode of operation;

FIG. **4** is the circuit of FIG. **3** redrawn to help determine the source impedance presented to the emitter; and

FIG. **5** is a schematic circuit diagram of a preferred embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

With reference now to the drawing and more particularly FIG. 1 thereof, there is shown a schematic circuit diagram of an embodiment of the invention for providing gain between input terminal **11** and output terminal **12** while matching a source impedance R_s connected to input terminal **11** and a load impedance R_L connected to output terminal **12**. The circuit comprises transistors Q1 and transformer T1. So as not to obscure the principles of the invention the specific means for applying operating and biasing potentials to the particular circuit elements are not shown, those skilled in the art knowing how to supply these potentials. For example, the collector may recieve d-c operating potential through the secondary winding of transformer T1 from a d-c supply bypassed to ground by a suitable capacitor in a manner well-known in the art.

For convenience in the explanation which follows below input terminal **11**, output terminal **12**, the emitter and the collector are designated nodes *a*, *b*, c and *d*, respectively. The primary winding **13** is connected between input terminal **11** and the emitter. The secondary winding of transformer T1 has a tap **14** connected to output terminal **12** and a first portion **15** between tap **14** and ground, reference or common terminal **16** and a second portion **17** between tap **14** and the transistor collector. The base of transistor Q1 is effectively connected to ground terminal **16**. The winding polarities are indicated by the dots.

Referring to FIG. **2**, transistor Q1 is represented as an ideal common base circuit having an input admittance y_{11} between base and emitter that is infinite, and output admittance y_{22} between collector and ground that is zero, a reverse transfer admittance y_{12} that is zero and a ratio of forward transfer admittance y_{21} to input admittance y_{11} that is unity.

Referring to FIG. **3**, there is shown an ideal equivalent circuit of the amplifier with a source resistance R_s connected between input terminal 11 and ground **16**, a load resistance R_L connected between output terminal 12 and ground **16**, and transistor Q1 represented as an ideal current source **21** connected between ground **16** and node d delivering the same current i_a into node *d* that enters node a and produces a potential v_a across primary winding **13**. Voltages across portions **17** and **15** and the currents flowing in the various leads are as indicated in FIG. **3**.

The following relationships hold:

$$v_m = nv_a \tag{1}$$

$$v_m = mv_a \tag{2}$$

$$i_a + ni_a = mi_m \tag{3}$$

Since a flows through both the single primary turn and the n turns, then

$$i_m = [(1+n)/m]\ i_a$$

With the transformer ideal, and the dependent current generator at node d, the following relationships hold:

$$v_b = mv_a \tag{4}$$

$$i_b = -(i_a + i_m)$$

$$i_b = -[(m + n + 1)/m]\ i_a \tag{5}$$

Hence

$$v_b i_b = -(m + n + 1)\, i_a v_a \tag{6}$$

$$v_b/i_b = -[m^2/(m+n+1)]\ v_a/i_a \tag{7}$$

With a voltage source in series with source resistance R_s, i_b flows outward into R_L, and

$$v_b/i_b = -R_L \tag{8}$$

Hence from (7)

$$v_a/i_a = [(m+n+1)/m^2]\ R_L = R_{in} \tag{9}$$

With a voltage source in series with R_L, i_a flows outward into R_s, and

$$v_a/i_a = -R_s \tag{10}$$

Hence from (7)

$$v_b/i_b = [m^2/(m+n+1)]R_s = R_{out} \tag{11}$$

The input impedance matches the source resistance R_s if m and n are related by

$$R_{in} = R_s = [(m+n+1)/m^2]R_L \tag{12}$$

If this expression for R_s is substituted in equation (11), $R_{out} = R_L$, the desirable situation of two-way impedance match. Rewriting equation (12) to relate m and n for two-way impedance match,

$$n = m^2(R_s/R_L) - m - 1 \tag{13}$$

Note that if m is an integer and R_s and R_L are related so that $m^2(R_s/R_L)$ is also an integer, then n will also be an integer.

It is assumed that equation (13) is satisfied from here on. With a voltage source, v, in series with R_s, then the available power at the input is

$$P_{av_a} = v^2/4R_s \tag{14}$$

But with equation (13) satisfied, the input is matched and

$$v_a = v/2 \text{ and } P_{av_a} = v_a i_a \tag{15}$$

The power delivered to the load at node b is

$$P_b = -v_b i_b = (m+n+1)\ P_{av_a} \tag{16}$$

The transducer gain G is the ratio of:

$$P_b/P_{av_a} = G = m+n+1 = m^2(R_s/R_L) \tag{17}$$

Likewise with the generator at node b we have

$$P_{av_b} = v^2/4R_L,\ v_b = v/2 \text{ and } v_b i_b = P_{av_b}$$

Hence:

$$P_a = -v_a i_a = [1/(m+n+1)]P_{av_b} \tag{18}$$

and the reverse gain G_r is given by

$$P_a/P_{av_b} = G_r = 1/G \tag{19}$$

With the source at node a the load impedance, R_{Lc}, presented to the collector is

$$R_{Lc} = v_a/i_a = [(n+m)\ v_a]/i_a \tag{20}$$

but $v_a/i_a = R_s$. Hence:

$$R_{Lc} = (n+m)\ R_s \tag{21}$$

Referring to FIG. 4, the equivalent circuit of FIG. 3 is redrawn to facilitate determining the source impedance presented to the emitter as seen looking in at the emitter feed point between node c and ground 16. Assuming that node c is positive with respect to ground, the voltages and currents are as indicated in FIG. 4 and the following relationships occur.

$$R_{ec} = v_c/i_a = [v_a + (v_a/m)]/i_a \tag{22}$$

$$v_a = i_a R_s;\ v_b = i_b R_L \tag{23}$$

$$i_b = [(m+n+1)/m]i_a \quad (24)$$

Hence:

$$R_{ae} = R_s + [(m+n+1)/m^2]R_L \quad (25)$$

But comparing equation (12) with equation (25) shows that

$$R_{ae} = 2R_s \quad (26)$$

In summary for two-way impedance match the following relationships occur:

Turns Ratio:	$n = m^2 (R_s/R_L) - m - 1$	(13)
Forward Gain:	$G = m^2 (R_s/R_L)$	(17)
Reverse Gain:	$G_r = 1/G$	(19)
Collector Load Impedance:	$R_{Lc} = (n+m) R_s$	(21)
Emitter Source Impedance:	$R_{se} = 2R_s$	(26)

Referring to FIG. **5**, there is shown a schematic circuit diagram of a preferred embodiment of the invention showing typical parameter values. The same reference symbols identify corresponding elements throughout the drawing. FIG. **5** includes an input coupling capacitor **22**, an output coupling capacitor **23**, an emitter biasing resistor **24** in series with an *r-f* choke **25**, biasing resistors **26** and **27**, bypass capacitors **31** and **32** and B+ terminal **33**. The circuit dissipates negligible *r-f* power. Resistors **24**, **26** and **27** do not dissipate *r-f* power because negligible *r-f* current flows through them. Were transformer **T1** and transistor **Q1** ideal and lossless, there would be essentially no *r-f* power loss between input and output. Because of the nature of the circuit, the circuit dynamic range corresponds substantially to that of transistor **Q1**.

With the circuit of FIG. **5** and **10** ma. delivered into terminal **33** at 15 volts, the invention had a gain of 8dB± 0.25 dB from 5 to 350 MHz. For input and output impedance of 50 ohms the maximum VSWR was 1.5 from 5 to 100 MHz and 2 from 100 to 250 MHz. The maximum noise figure was 1.2 dB from 5 to 150 MHz and 1.5 dB from 150 to 200 MHz. The minimum power output at 1dB compression over 5 to 150 MHz was 10 dBm and from 150 to 200 MHz **9** dBm.

There has been described a novel *r-f* amplifying circuit characterized by matching source and load impedances and good amplification over a relatively broad bandwidth while using relatively few components, components that need not be adjusted and are relatively economical. It is evident that those skilled in the art may now make numerous uses and modifications of and departures from the specific embodiments described herein without departing from the inventive concepts. Consequently, the invention is to be construed as embracing each and every novel feature and novel combination of features present in or possessed by the apparatus and techniques herein disclosed and limited solely by the spirit and scope of the appended claims.

What is claimed is:

1. Amplifying apparatus comprising,
amplifying means having at least control, input and output electrodes,
a common terminal,
transformer means having at least a primary and a secondary winding,
said secondary winding having a tap intermediate to first and second portions thereof,
an input terminal,
an output terminal,
means for coupling said output terminal to said tap,
means for coupling said primary winding between said input terminal and said input electrode,
said first portion being coupled between said tap and said common terminal,
said second portion being coupled between said tap and said output electrode,
and means for coupling said control electrode to said common terminal.

2. Amplifying apparatus in accordance with claim **1** wherein the turns ratio between said first portion and said primary winding is m and between said second portion and said primary winding is n with $n = m^2 R_s/R_L - m - 1$ wherein R_s is a predetermined source resistance and R_L is a predetermined load resistance.

3. Amplifying apparatus in accordance with claim **2** and further comprising said source resistance coupled between said input terminal and said common terminal and said load resistance coupled between said output terminal and said common terminal.

4. Amplifying apparatus in accordance with claim **1** wherein said amplifying means comprises a transistor and said control, input and output electrodes comprise base, emitter and collector electrodes, respectively.

5. Amplifying apparatus in accordance with claim **4** and further comprising,
a source of d-c operating potential connected to said collector electrode through said secondary winding,
and means for biasing said base and emitter electrodes.

6. Amplifying apparatus in accordance with claim **5** wherein the means for biasing said base electrode comprises a first resistor connected between said source of d-c potential and said base electrode and a second resistor connected between said base electrode and said common terminal and the means for coupling said base electrode to said common terminal comprises an *r-f* bypass capacitor and further comprising,
another *r-f* bypass capacitor coupling said source of a d-c potential to said common terminal.

7. Amplifying apparatus in accordance with claim **6** wherein said means for biasing said emitter electrode comprises an emitter biasing resistor in series with an *r-f* choke between said common terminal and said primary winding.

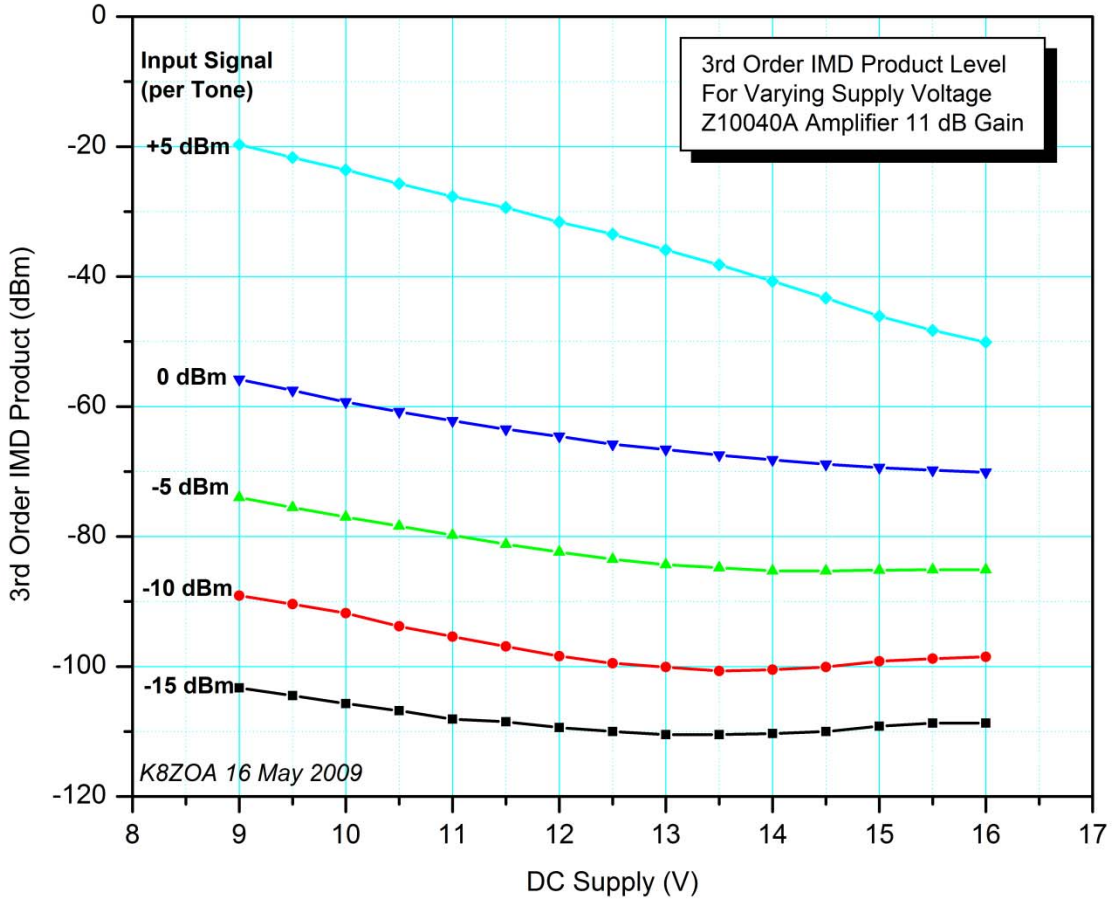
8. Amplifying apparatus in accordance with claim **7** wherein said means for coupling said primary winding between said input terminal and said emitter electrode comprises a capacitor and said means for coupling said output terminal to said tap comprises a capacitor.

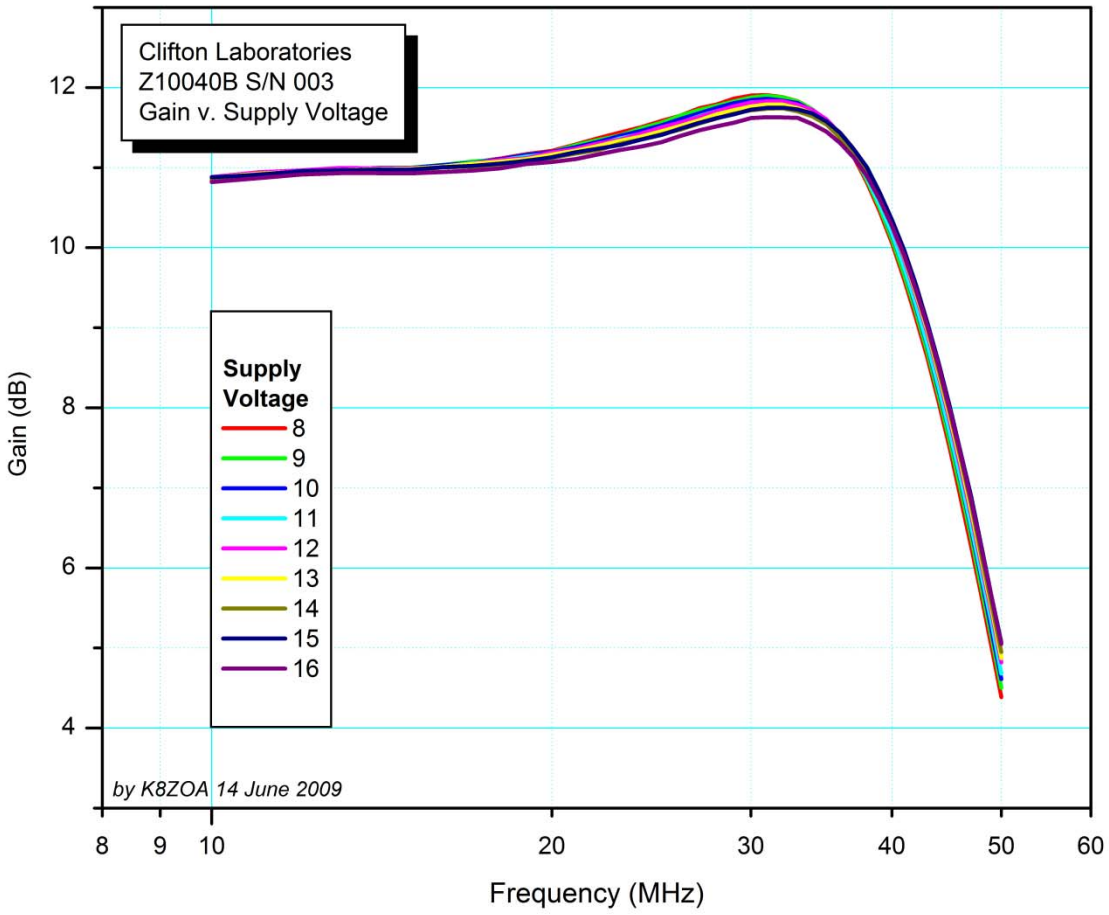
* * * * *

Appendix D IP3, Noise Figure and Gain Performance versus Operating Voltage

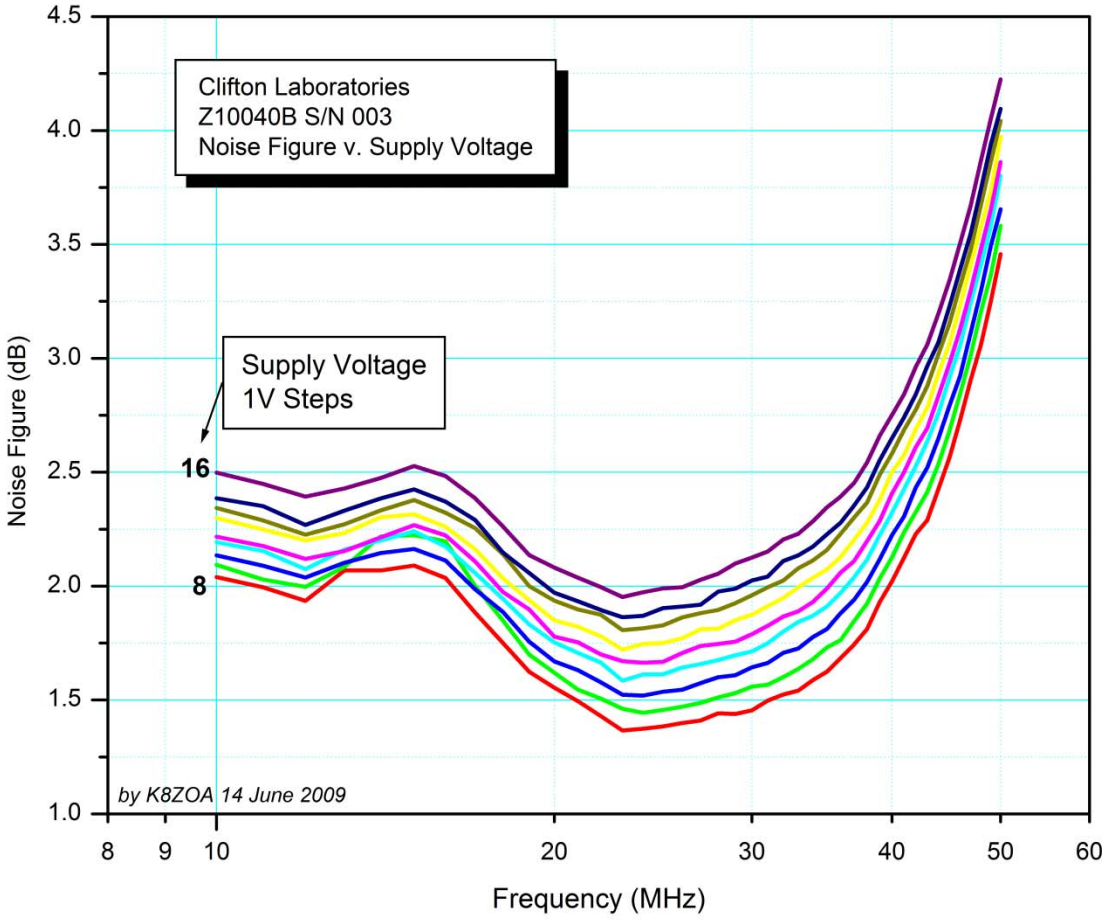
The recommended range of operating voltages for the Z10040B is 13.8V minimum, 15V maximum. The primary limiting factor is heat dissipation of the 2N5109 transistors, particularly when operated outdoors in a shielded enclosure in a hot climate. Under certain circumstances, however, it may be desirable to operate with considerably lower voltage levels.

The figure below shows the typical change in 3rd order intermodulation performance for a Z10040A amplifier—the Z10040B will behave in a similar fashion. For typical signal levels found on an antenna, there's a reasonably broad point of optimum performance for supply voltages between 13 and 15V. The vertical axis in the plot is the level of 3rd order intermodulation products as a function of input signal level and operating voltage. The lower the 3rd order intermodulation product for a given input signal level, the better the amplifier performance.





The figure above shows the relationship between supply voltage and gain for a typical Z10040B amplifier. As expected for an amplifier employing negative feedback, gain is essentially independent of supply voltage.



The figure above shows the measured noise figure of a typical Z10040B amplifier with supply voltage ranging from 8 to 16 volts. The data shows a clear pattern of lower supply voltage corresponding to better noise figure, with the difference between 8V and 16V being around 0.5 to 0.7 dB at frequencies between 10 and 30 MHz.

In the circumstances where best noise figure is more important than intermodulation performance, therefore, operation with supply voltages of 10V or less may be useful.

The data presented is believed representative of typical Z10040B amplifiers, but due to unit-to-unit variation, the performance levels presented as "typical" and are not warranted.

As a matter of prudence, particularly where the amplifier is operated inside a shielded enclosure in elevated ambient temperature, Clifton Laboratories recommends 13.8 as the supply voltage. If used indoors in a climate-controlled environment, a somewhat greater supply voltage may be used, although exceeding 14 to 14.5 volts is almost certainly unnecessary and should only be done with a clear understanding of the risks of overheating and damaging Q1 and Q2.

Appendix E Manual Backdating

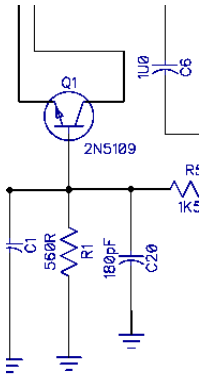
14 June 2009.

The Z10040B Norton Amplifier can exhibit instability evidenced by parasitic oscillations in the 650 MHz range. The instability is associated with a combination of:

- Q1 and Q2 having significantly above average gain;
- Heat sink orientation maximizing Q1-Q2 coupling; and
- Unbalanced input with one particular input pin grounded.

Changes to stabilize the Z10040B under these conditions were added on this date. The changes are:

1. Heat sink orientation to reduce mutual capacitance between Q1 and Q2.
2. When using unbalanced input, connect the coaxial cable so that the center conductor mates with pin 2 and the shield connects to pins 1 and 3. Pin 4 may be left unconnected. <u>Do not use a connection that places the shield on J1, pin 2 and the center conductor on J1, pin 3</u>.
3. Added C20, 180 pF ceramic capacitor to Q1 base to ground. C20 is mounted on the PCB's bottom surface.



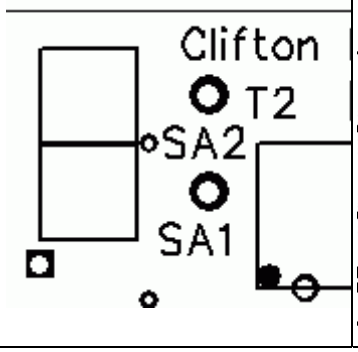
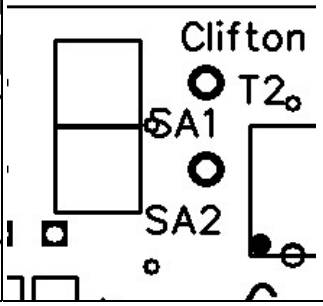
Errata:

1. The silk screen identifiers for SA1 and SA2 are reversed.
2. T2 and T4. Silk screen identifiers for pads D and E are reversed.

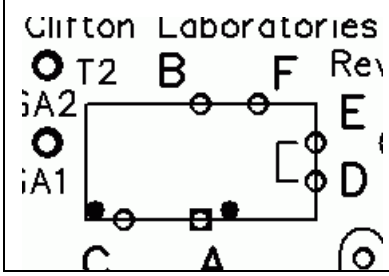
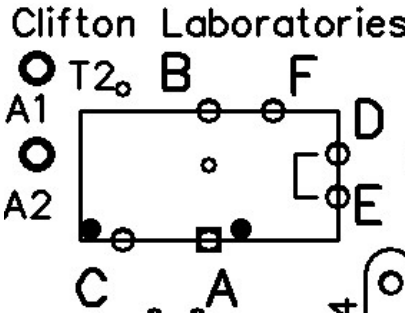
29 August 2009

Revision 02 printed circuit board introduced. The rev 02 PCB makes several changes:

<u>Corrected error in SA1 and SA2 silk screen</u>

Rev 1 board with reversed silk screen legend for SA1 and SA2	
Rev 02 board corrected SA1 and SA2 silk screen.	

Revised identification for pads D and E in transformers T2 and T4

Rev 01 board	Rev 02 board
	

Pads D and E are electrically connected together. The change in rev 2 makes no change in connectivity but conforms the printed circuit board silk screen to the transformer winding instructions.

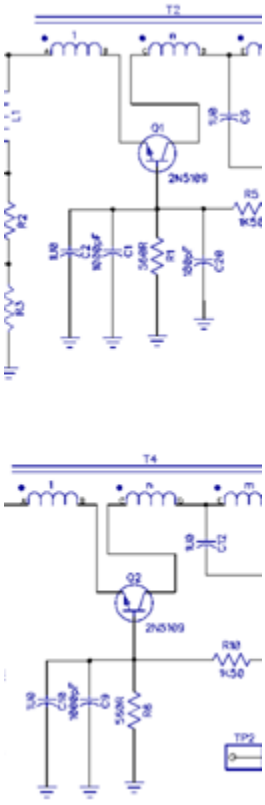
Parts Changes

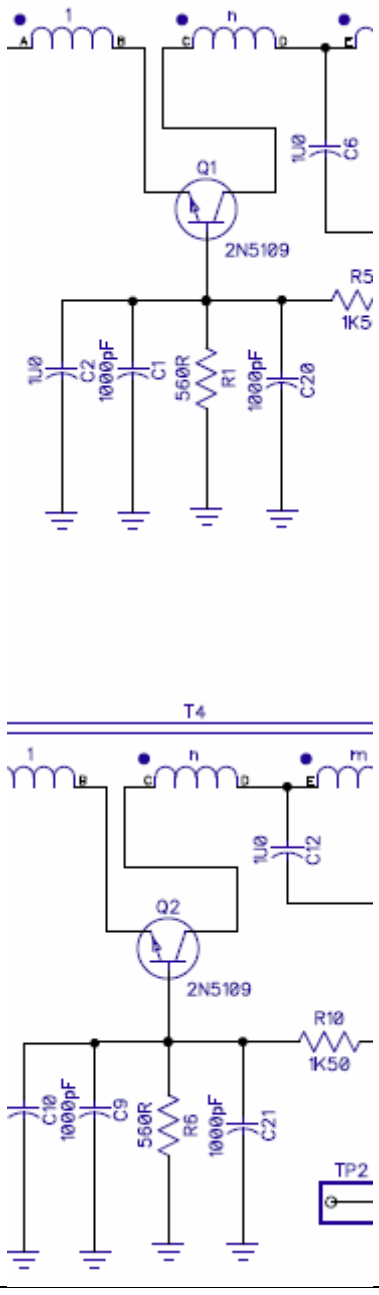
Spacer for L1-L4 may be either nylon or hard fiber.

In rev 01, C20 was 180 pF, through-hole type installed on the PCB bottom. In rev 02, C20 and new C21 are now 1000pF 1206 surface mount parts, installed on the PCB bottom.

Improved Symmetry for Q1 and Q2

Rev 01 added a 180 pF stability bypass capacitor to Q1's base. No similar change was made to Q2.	Rev 02 improves symmetry by adding stability bypasses to both Q1 and Q2. The bypass value has been increased to 1000pF and the parts are surface mount, installed on the PCB's bottom.





23 November 2009

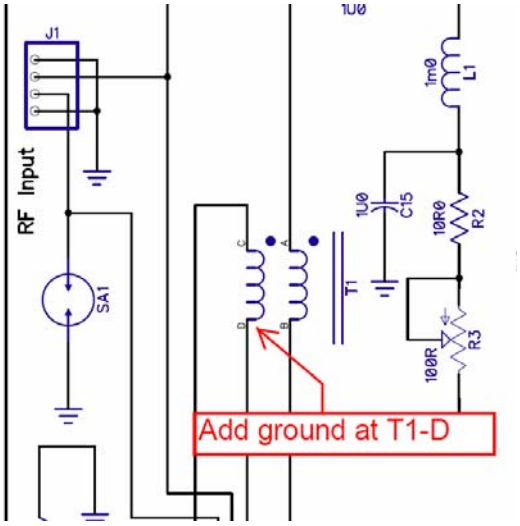
C20 & C21 changed to 100pF. Units assembled with other values need not be modified, as this change is mainly for compatibility in parts stock with other Clifton Laboratory kits.

16 January 2010

Two changes were introduced.

Unbalanced Input Optional Modification

At the request of some customers, the Z10040B added optional balanced input (the Z10040A was unbalanced input only), with the choice between balanced and unbalanced operation being made via input plug location. If the Z10040B is to be used only in unbalanced mode (which is likely to be the vast majority of cases) a slight improvement in performance can be observed by adding a grounding point near T1's pin "D."



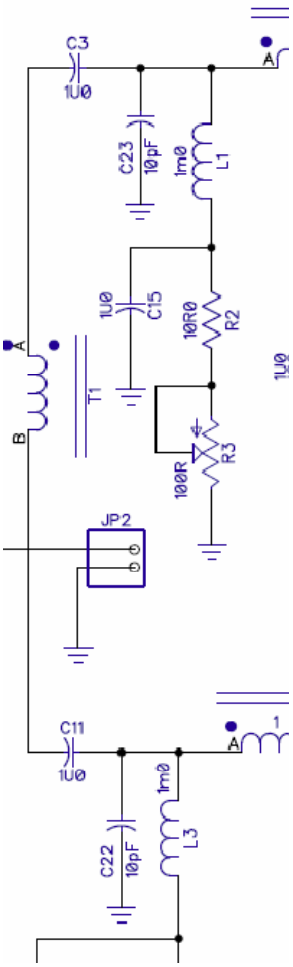
This manual now has an optional procedure to install a direct ground connection at T1, pin D.

Stability modification where Q1 & Q2 have unusually high gain at UHF

Part of the Z10040B's kitting process is to measure the DC gain (H_{FE} or beta) of all 2N5109 transistors and group them into matched pairs. Usually the measured beta runs between 40 and 80. The lot of 2N5109 transistors received in mid January 2010, however, showed beta values between 120 and 160. The greater DC gain also translated into higher gain at UHF frequencies, with a resulting parasitic oscillation around 900 MHz under certain conditions of input and output termination.

The solution is to roll off the gain by adding capacitors C22 and C23 (10pF) to the input circuit. This small capacitance does not alter performance within the Z10040B's normal operating range, but it is sufficient to provide stability with the highest gain 2N5109 transistors available to me (beta > 170.)

C22 and C23 are 10pF disc ceramic capacitors installed on the bottom PCB surface.



March 2010

Following text removed:

> Locate the remaining length of No. 24 AWG magnet wire and cut two lengths 1.25 inch (32 mm) long. These will be the single turn winding A-B. Strip and tin each end approximately 0.25 to 0.375 inches (6.5 mm to 9.5 mm) and install between pads A and B, passing the wire through the transformer's central hole. Installing this wire will be easier if you first install the wire vertically (not passed through the core) in the pad away from the board edge. Solder the wire in place. Then pass it through the transformer core and into the outside pad hole. Solder.

The one-turn transformer windings use a short length of Teflon insulated solid wire. This change is to provide a more secure physical mounting for the two transformers.

Revised 2nd and 3rd order Intermodulation specifications and measurement protocol to reflect 3 & 4 MHz test tones at 0 dBm output, to bring the Z10040B into conformity with intermodulation specifications of other Clifton Laboratories products.

Several small cosmetic changes and clean up steps were also made.

April 2010

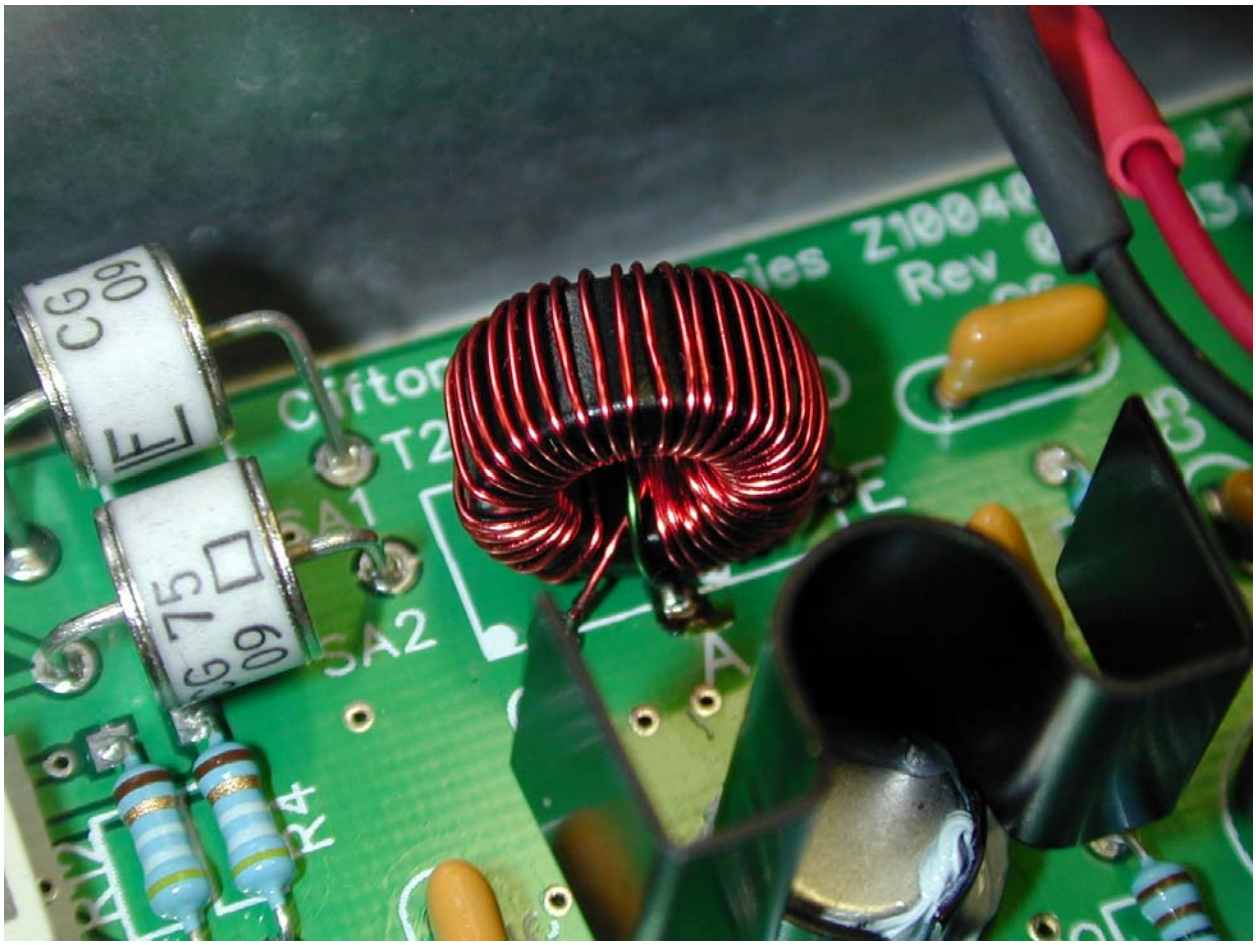
Based upon customer build experience, added a caution to winding T2 and T4; the winding orientation must be followed. It is not sufficient to make T2 and T4 match if they are wound in reverse. This is because windings A-B have a polarity ("dot notation") fixed by the printed circuit board layout. All other windings must be wound as shown in the illustration or else their polarity will be wrong with respect to windings A-B. The symptom of reversed winding orientation is oscillation, possibly at a high level (0 dBm or greater.)

Appendix F Z10040B Performance Increased Gain

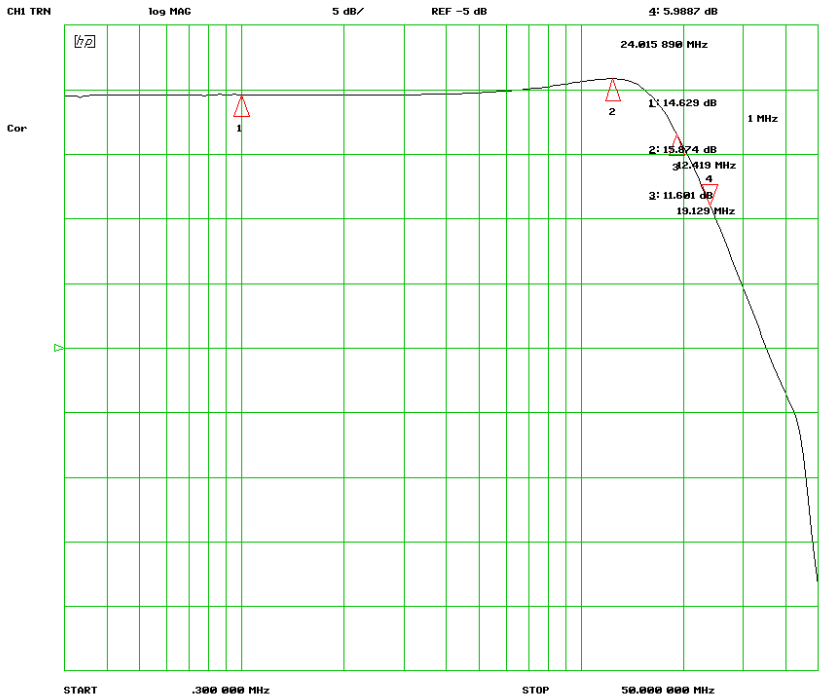
This appendix describes the performance changes when a Z10040B is built with a 1:29:6 turns ratio. The data provided is from a sample of one amplifier and while believed accurate, some unit-to-unit variation may be expected.

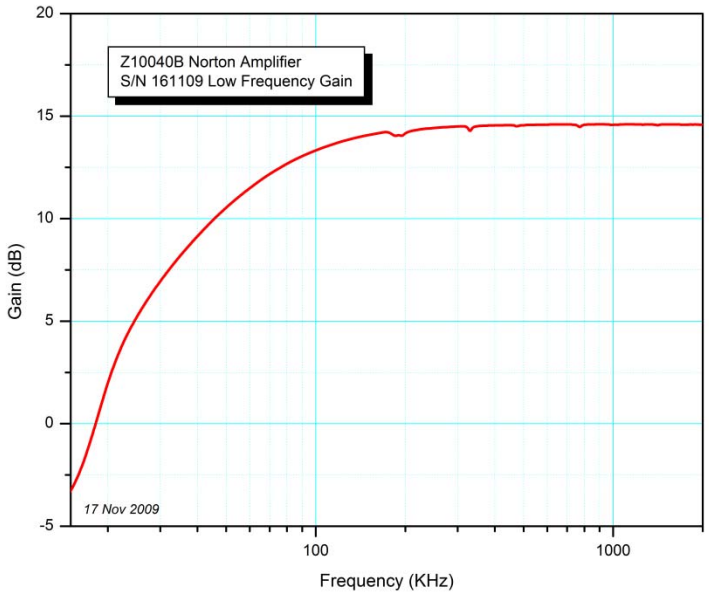
As discussed earlier in this manual, a Norton amplifier's gain is defined by the transformer (T2 and T4) turns ratio, with the "normal" Z10040B being constructed with a 1:11:4 turns ratio. From the Norton patent, the theoretical gain when built with a 1:29:6 turns ratio is $20*\log_{10}(6)$ or 15.6 dB. In practice, a dB or so loss from theoretical gain should be added to reflect losses in the input and output transformers among other sources.

The illustration below shows T2 built with a 1:29:6 turns ratio. #24 AWG wire can be used, but as the photo shows, it's a tight fit.


T2
SA1
SA2
R4

As might be expected, increased gain comes at a price; the upper -3 dB point is significantly below the 1:11:4 standard Z10040B amplifier. The figure below shows 14.6 dB gain at 1 MHz, with the upper -3 dB point being 19.1 MHz. (The standard 1:11:4 Z10040B has an upper -3 dB point around 40 MHz.) The lower -3 dB point is 65 KHz, essentially unchanged from the standard 1:11:4 amplifier.





With respect to other key performance measures, the 1:29:6 version shows:

- 3rd order intermodulation intercept (output referenced) degrades to +32 dBm
- 2nd order intermodulation intercept (output referenced) degrades to approx. +90 dBm
- Noise figure is not materially different from the 1:11:4 version.